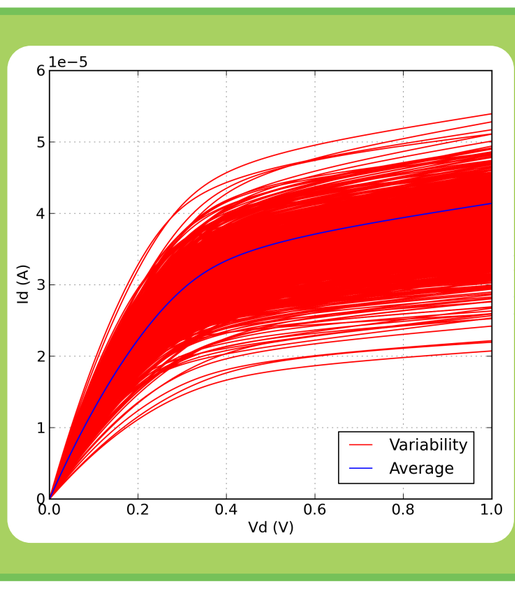
A RECONFIGURABLE ARCHITECTURE FOR CURRENT AND FUTURE CHALLENGES IN ELECTRONIC DESIGN AND TECHNOLOGY

The PAnDA Project
www.panda.ac.uk

Introduction

Great efforts are made to integrate more programmable logic into already complex, powerful FPGAs, but whenever there are tight constraints on bandwidth, power, speed and budget this is currently resolved by incorporating full-custom optimised building blocks rather than developing radically novel FPGA fabric structures. However, as device sizes are now approaching atomistic scales, intrinsic variations are becoming more abundant leading to lower production yield and higher failure rates. Particularly SRAM and latches are affected, which has a direct impact on FPGAs of which they are essential parts. In order to accommodate increased variability of individual devices, it is necessary to take a more holistic approach to electronic design, i.e. understanding and tackling problems on multiple levels rather than considering device, analogue, digital or system levels separately.

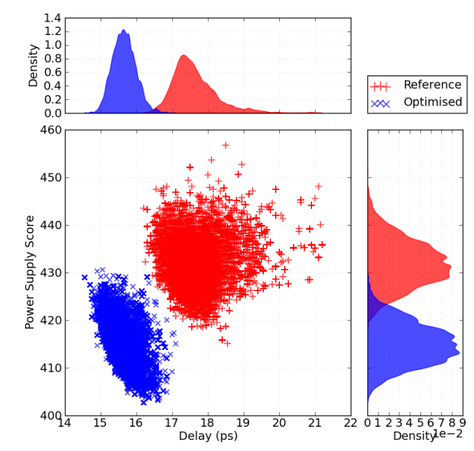


The PAnDA Project

The PAnDA (Programmable Analogue and Digital Array) project proposes a novel reconfigurable variability tolerant architecture,which allows variability aware design and rapid prototyping by exploiting mapping and configuration options at both the analogue and digital level. This is a novel approach to synthesizing designs on an FPGA, and is not possible with any currently existing commercial FPGA. This will enable us to investigate the optimisation of digital circuits on multiple layers of abstraction.

Optimising for Variability

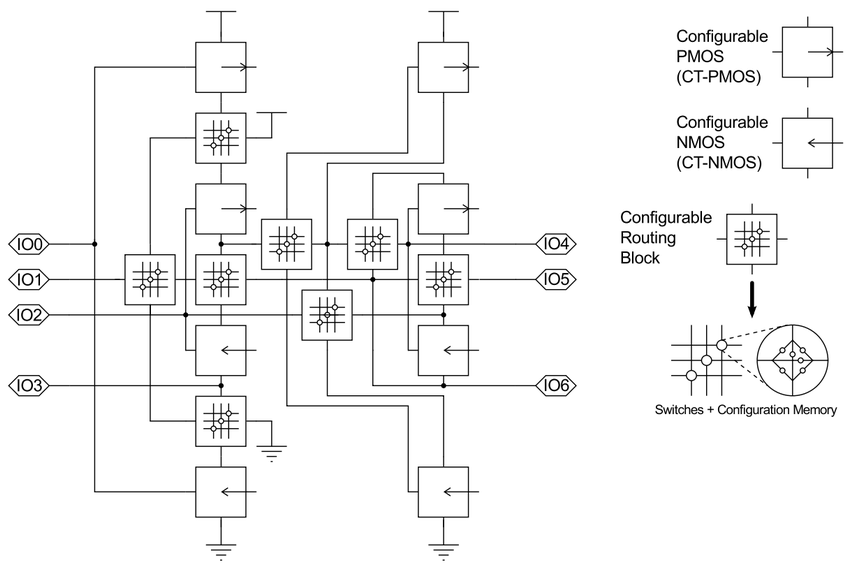
Previous research shows that optimising transistor dimensions of standard cell designs below 40nm using GSS' Randomspice and **ngenics** MOTIVATED technology may produce designs exhibiting reduced stochastic variability and improved performance (e.g. power consumption, delay).

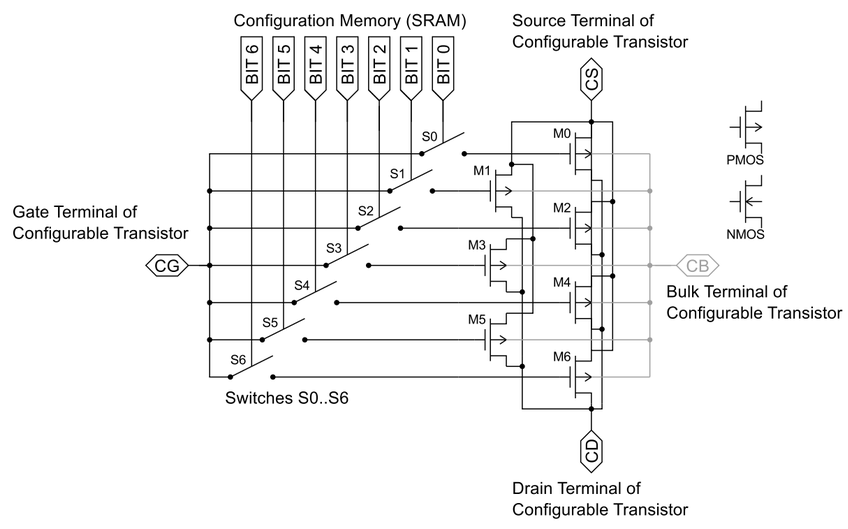


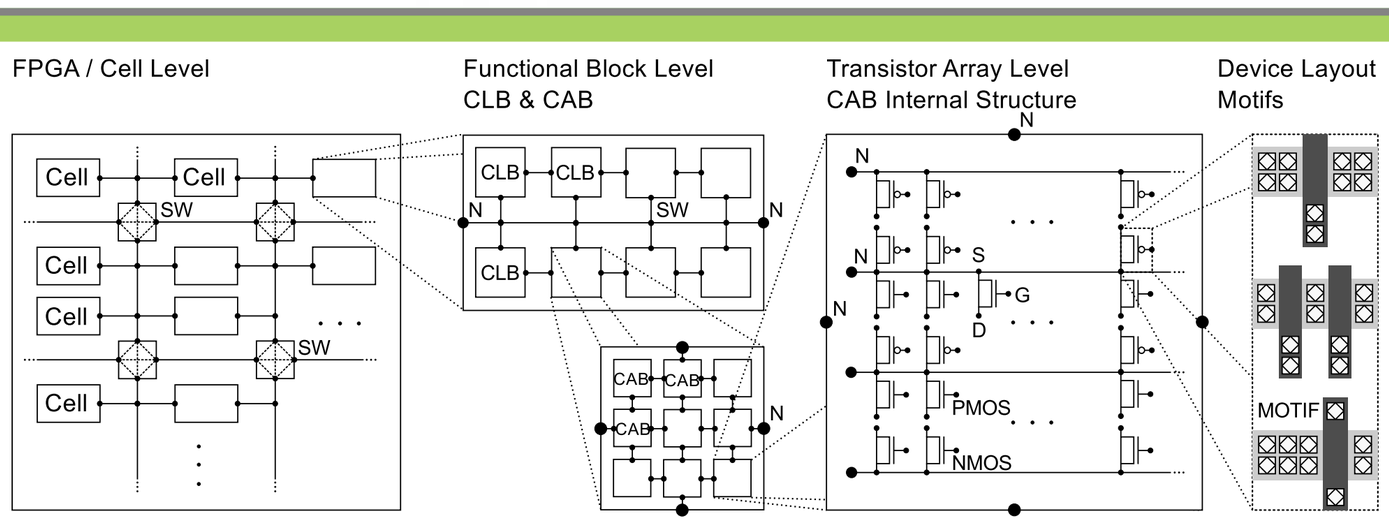
The PAnDA Architecture

PAnDA is a unique architecture encompassing novel Configurable Analogue Block (CAB) and Configurable Logic Block (CLB) designs. Each CAB contains PMOS and NMOS transistors, which can be configured to form SRAM and CMOS logic functions, representative of those found in standard cell libraries with different performance (e.g. power, speed) and variability tolerance characteristics. Each CLB contains a number of CABs, which can be configured to form larger logic blocks, such as Flip-flops and LUTs that are more commonly found in FPGA fabric.

The PAnDA architecture aims to close the gap between analogue standard cell design and digital systems design, by providing reconfiguration facilities on both the analogue and digital level. The focus is to configure PAnDA with digital designs and optimise them by changing location and topology of the digital components and by manipulating the properties and improving the intrinsic variability of parts of the circuit by changing the underlying analogue and device layers.







THE UNIVERSITY of York
DEPARTMENT OF ELECTRONICS

University of Glasgow

GSS

ngenics