UNIVERSITY OF Southampton
School of Electronics and Computer Science

An Energy-Efficient Radiation Hardened Register File Architecture for Reliable Microprocessors

Yang Lin, Mark Zwolinski and Basel Halak
Electronics and Electrical Engineering Group
School of Electronics and Computer Science
University of Southampton, UK
{yl5g09, mz, bh9}@ecs.soton.ac.uk

Presentation Overview

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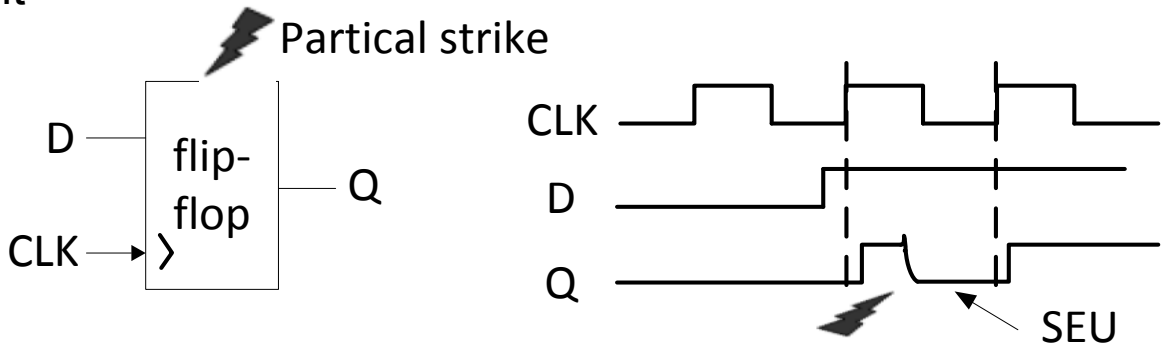
- Background
- Radiation Hardened Flip-Flop: SETTOFF
- Radiation Hardened Register File based on SETTOFF
- Failure Rate Evaluation Model
- Comparative Evaluation Results
- Conclusion

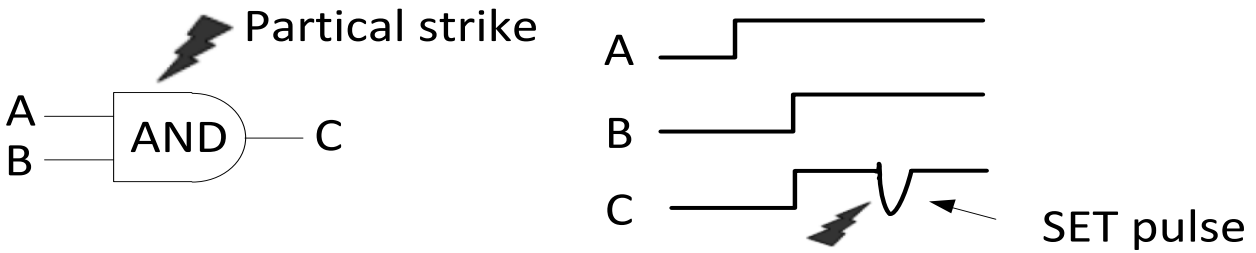
Background: Radiation-Induced Soft Error

***Soft Error*: A transient error induced by high-energy particle strikes**

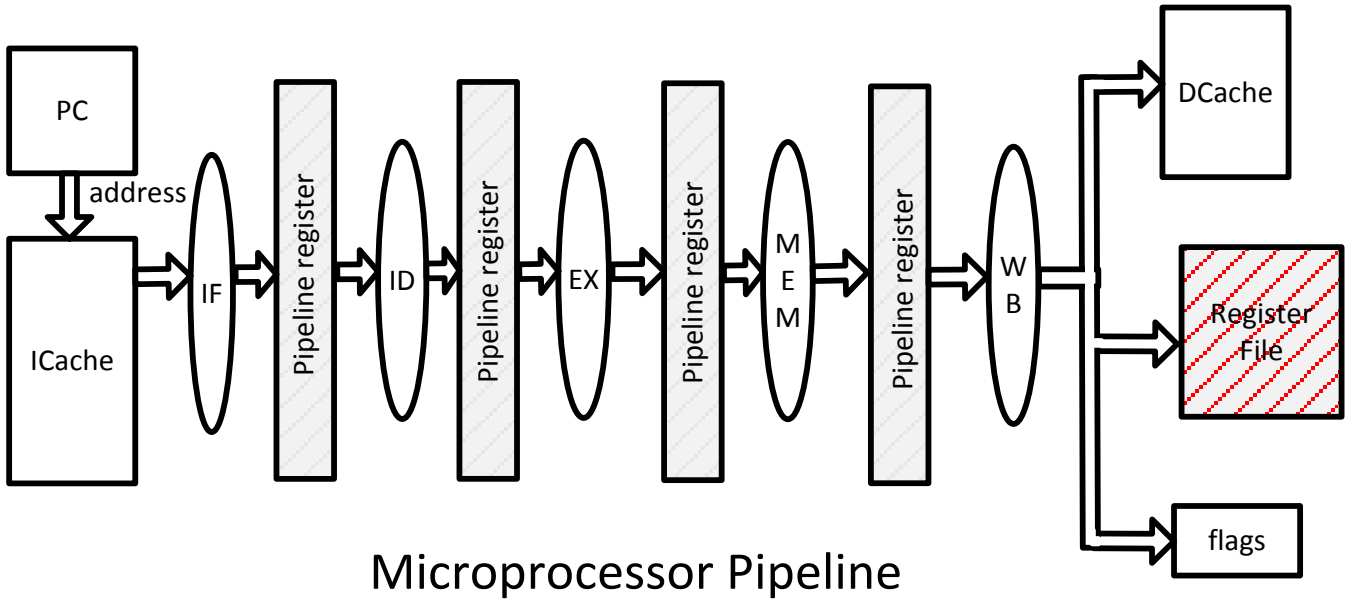
- SEU: Single Event Upset, a bit-flip error produced by the particle strike in sequential circuit



- SET: Single Event Transient a voltage pulse generated by the particle strike in combinational circuit.



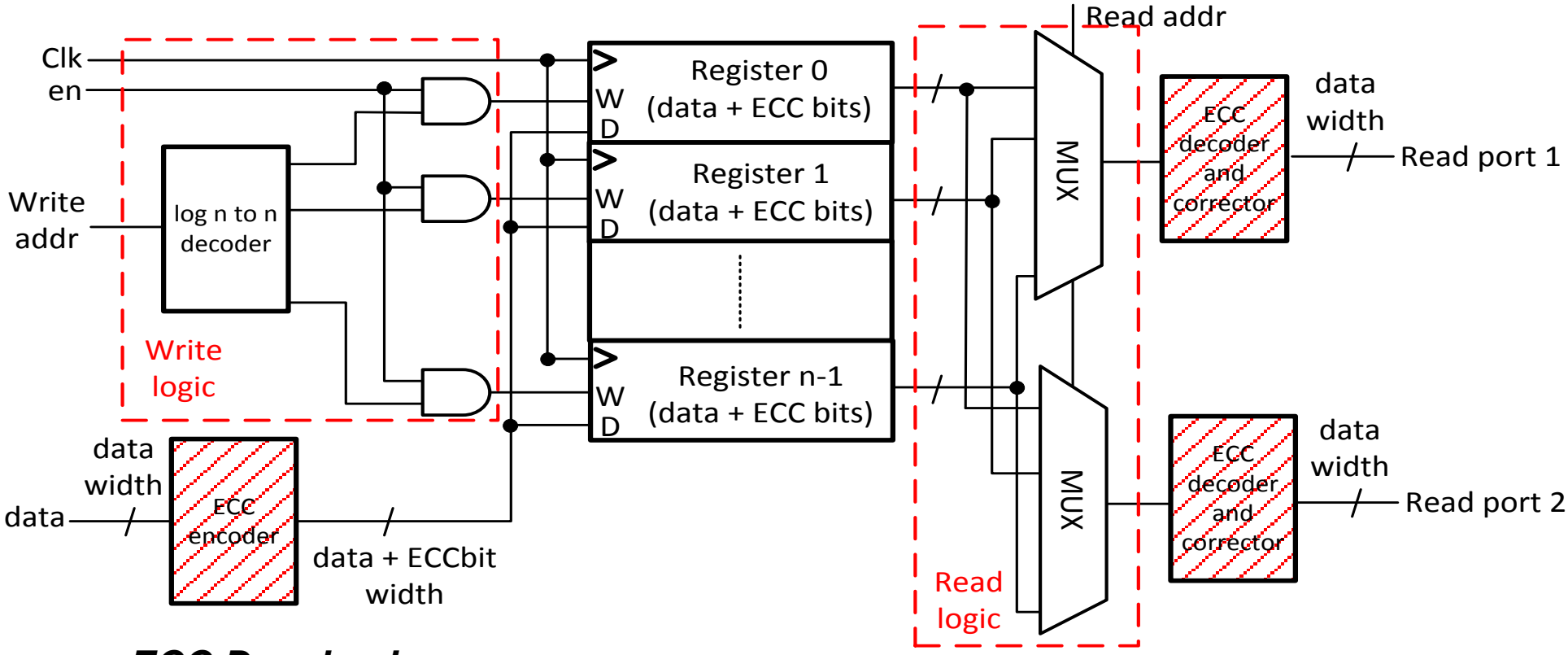
Background: Soft Error Vulnerability of Microprocessors



Microprocessor Pipeline

Register File (RF) is one of the most vulnerable parts since it stores the intermediate execution results of the processor and is frequently accessed. The errors occurring in the RF can easily propagate to other execution units and cause visible errors in final program results.

Background: ECC-based Register File Protection



ECC Drawbacks:

1.Addressing MBUs requires noticeably larger number of redundant bits.

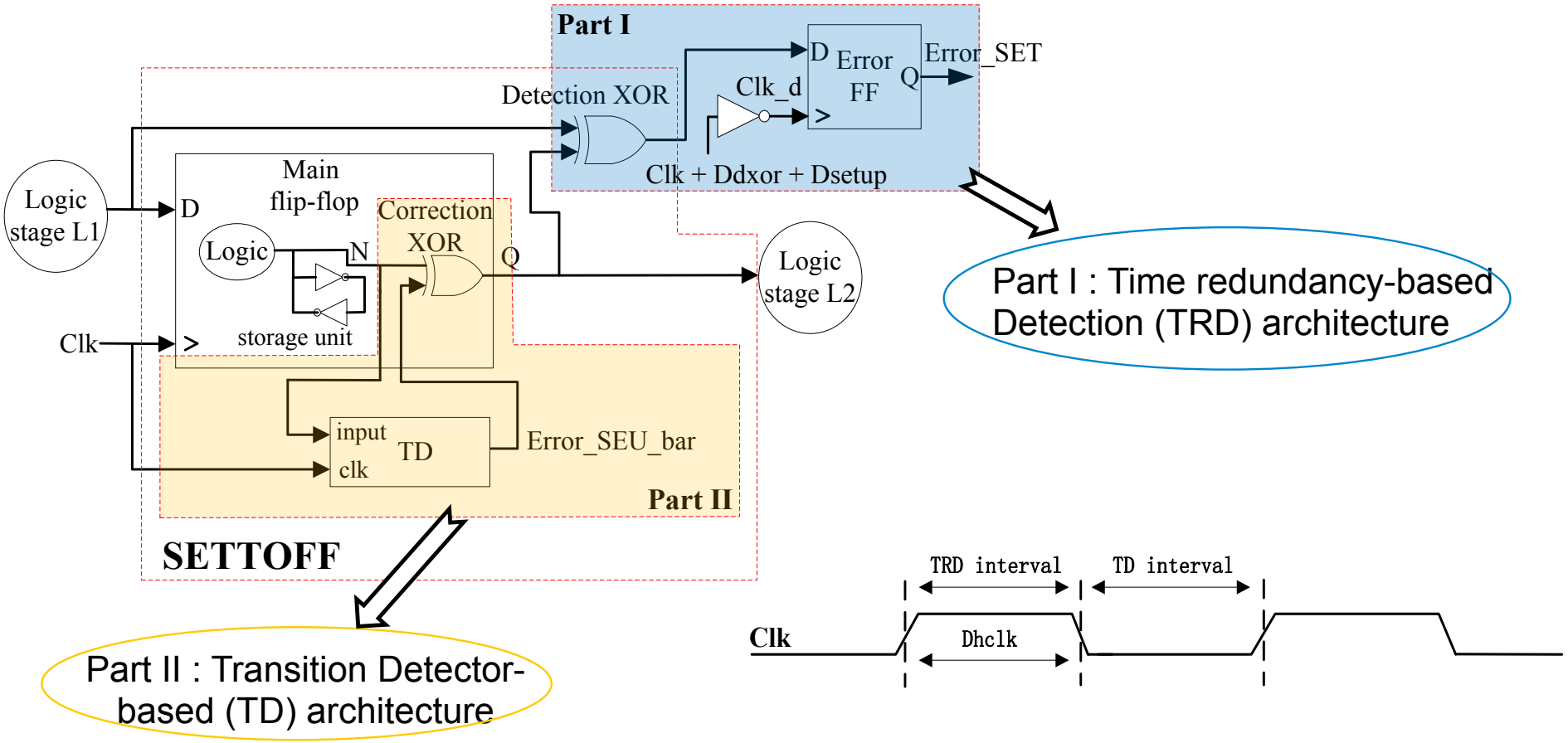
2.Big Power and delay overhead caused by the ECC encoder & decoder.

3.Can not address SETs, therefore the big write & read logic are not protected. (SETs have high probability to cause MBUs when captured)

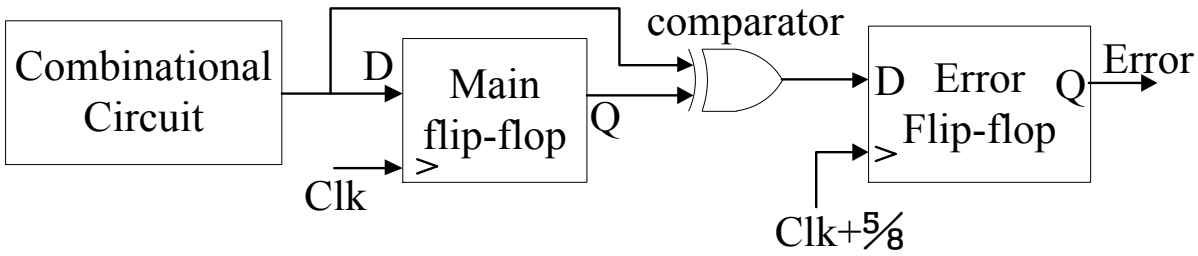
4.Multiple read ports require multiple ECC decoders.

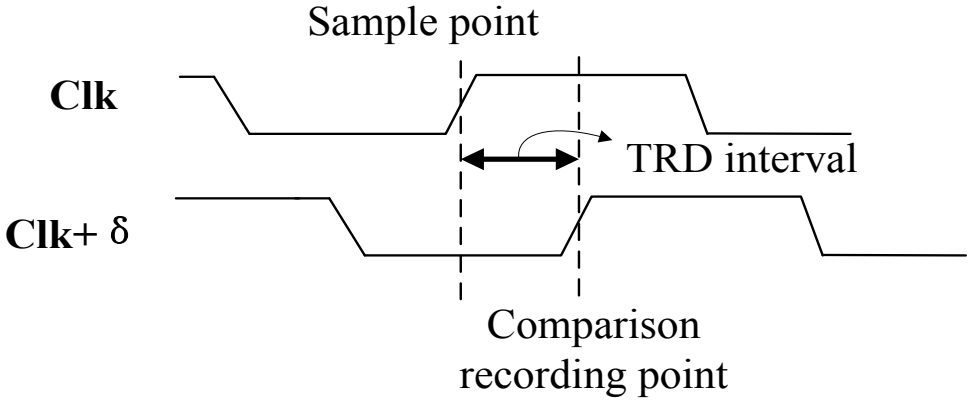
The architecture of SETTOFF

- SETTOFF: Soft Error and Timing error TOlerant Flip-Flop



Time Redundancy-based Detection (TRD)





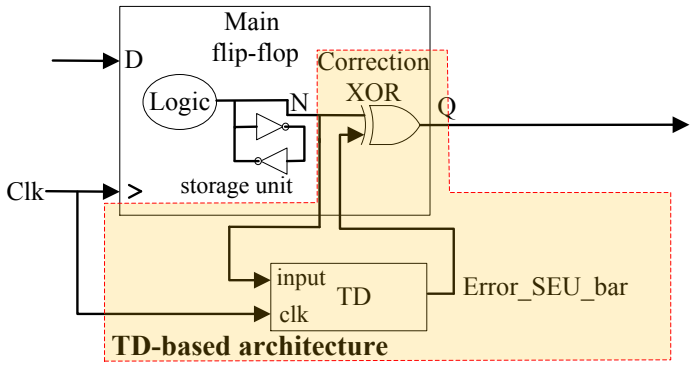
TRD can detect:

1.SETs with the width no greater than the TRD interval.

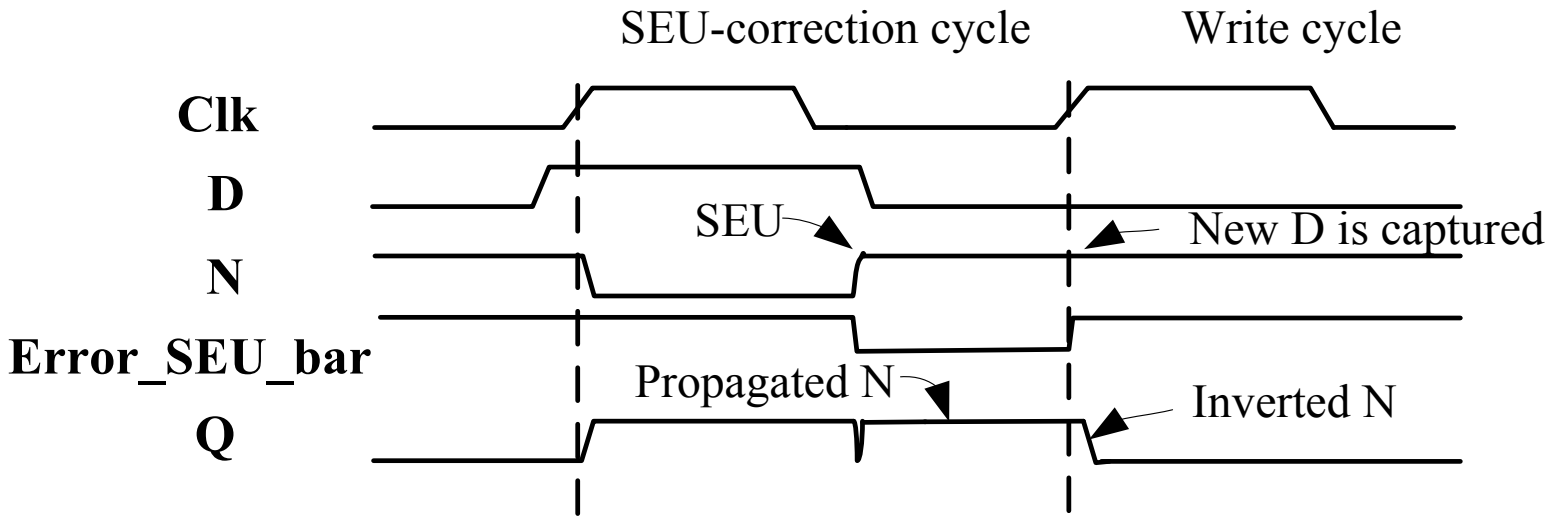
2.SEUs occurred within the TRD interval.

3. Timing errors.

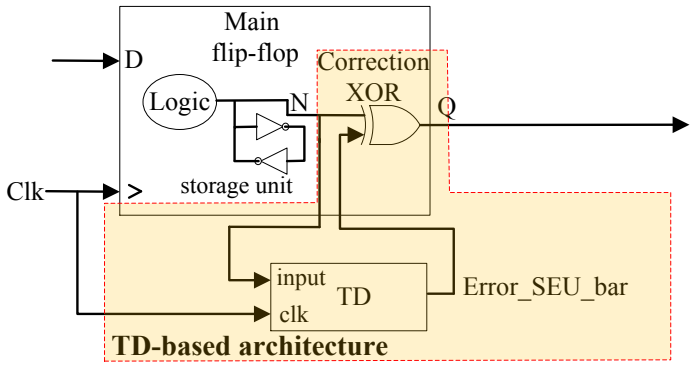
Operation of TD-based Architecture



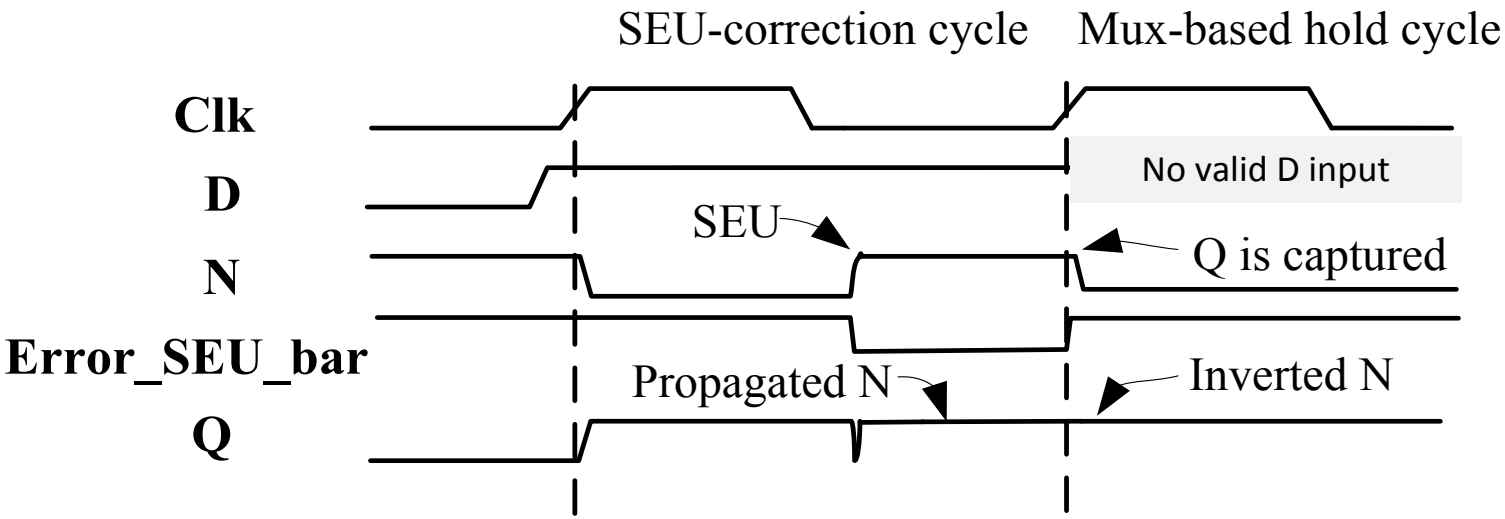
Case 1: A write cycle follows an SEU-correction cycle



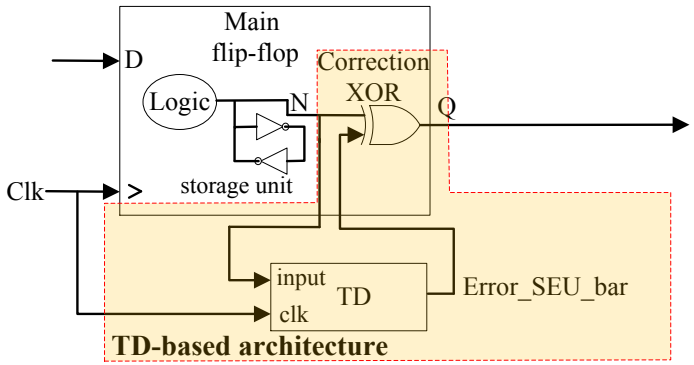
Operation of TD-based Architecture



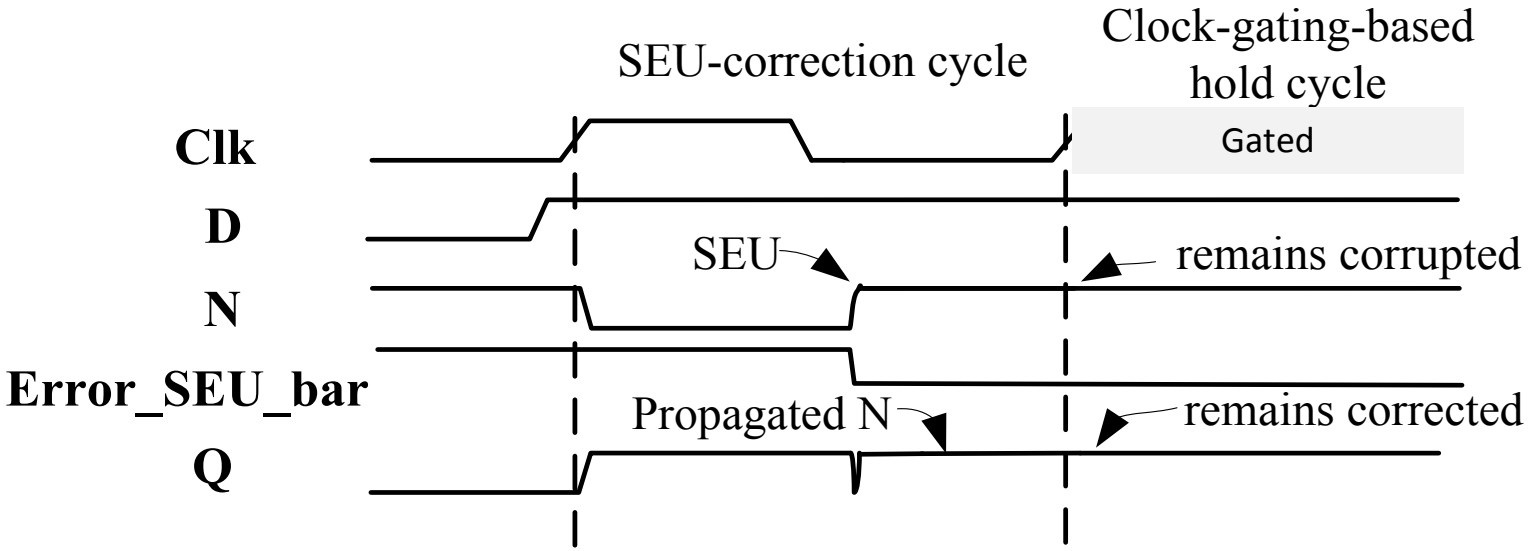
Case 2: A multiplexer-based hold cycle follows an SEU-correction cycle.



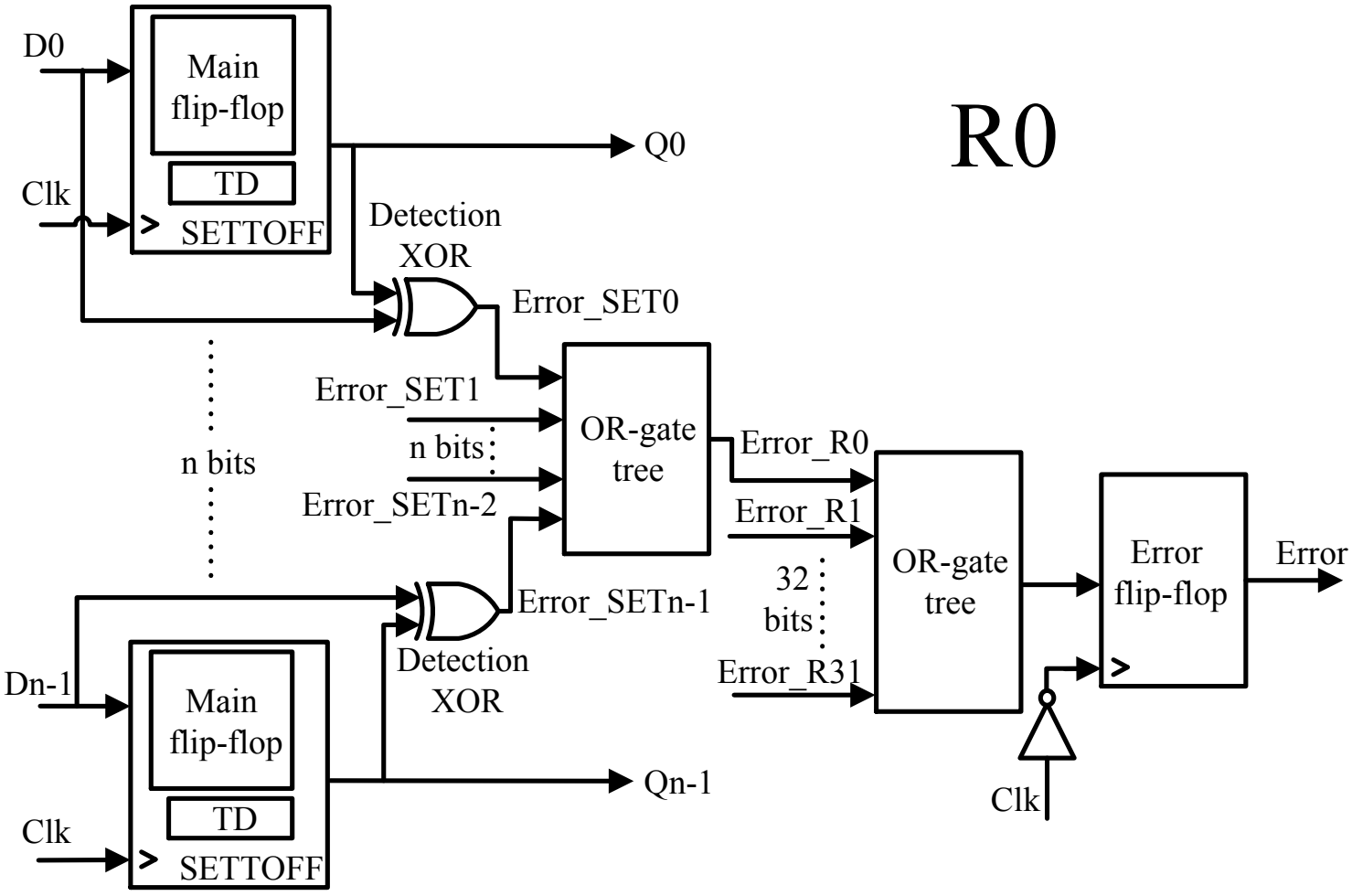
Operation of TD-based Architecture



Case 3: A clock-gating-based hold cycle follows an SEU-correction cycle.



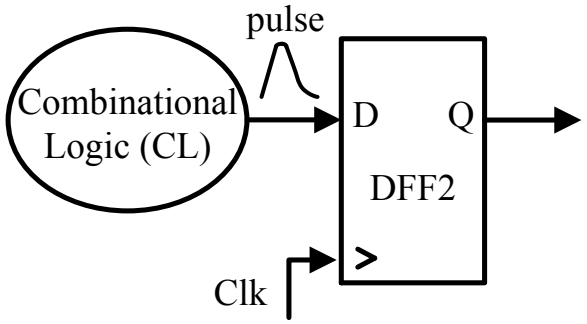
The SETTOFF-based Register File Architecture

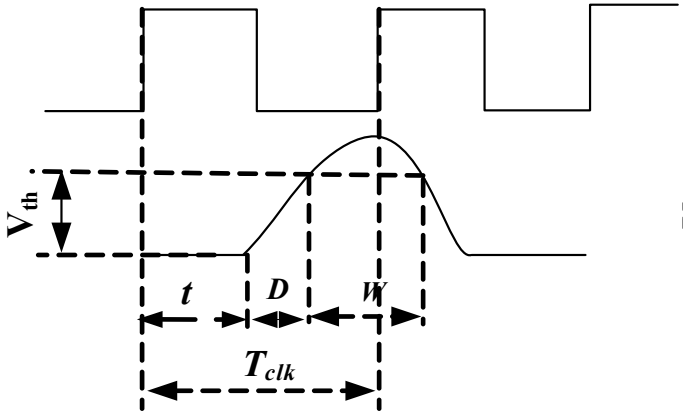


Soft Error Failure Rate Evaluation Model

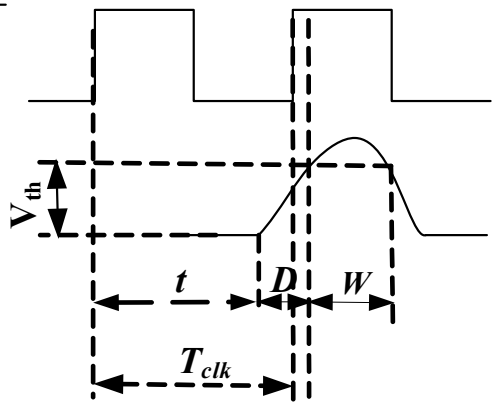
Failure of a flip-flop: The corruption of its output due to an SET or and SEU

SET failure rate for
Conventional flip-flops:





Scenario (1): Failure



Scenario (2): No Failure

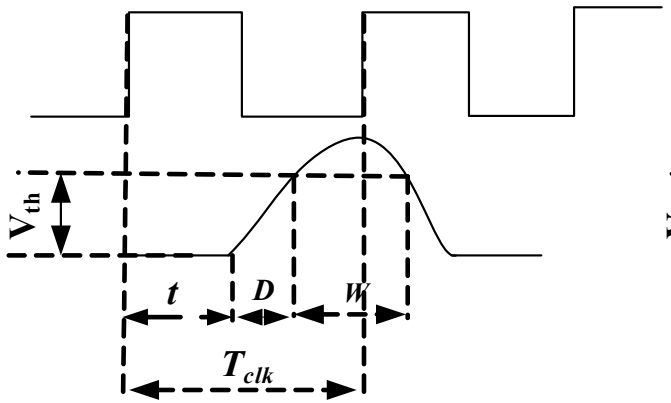
Probability of condition (1):

$$g1 = \Pr\left(T_{clk} \geq D + \alpha.T_{clk}\right) = \Phi\left(\frac{(\alpha-1)\mu_{T_{clk}} + \mu_D}{\sqrt{\sigma^2{}_D + ((\alpha-1).\sigma_{T_{clk}})^2}}\right)$$

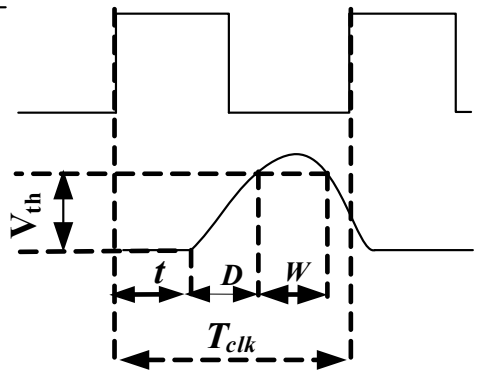
Where: $\alpha = t/T_{clk}$

SET Failure Rate Model for Conventional Flip-Flops

Two scenarios for condition (2):



Scenario (3): Failure



Scenario (4): No Failure

Probability of Condition (2):

$$g2 = \Pr\left(T_{clk} \le D + \alpha.T_{clk} + w\right) = \Phi\left(\frac{(1-\alpha)\mu_{T_{clk}} - \mu_w - \mu_D}{\sqrt{\sigma^2{}_w + \sigma^2{}_D + ((1-\alpha).\sigma_{T_{clk}})^2}}\right)$$

Failure rate for a conventional flip-flop: $Fr = g1 \cdot g2$

SET Failure Rate Model for SETTOFF

For SETTOFF, a SET pulse also has to satisfy 2 conditions to cause a failure. The first condition is the same as for a conventional flip-flop. However, the second condition requires the pulse amplitude to remain higher until the end of the TRD interval

$$g2' = \Pr(T_{clk} + T\tau_{clk} \le D + \alpha T_{clk} + w)$$

$$= \Phi\left(\frac{(1+\tau-\alpha)\mu_{T_{clk}} - \mu_w - \mu_D}{\sqrt{\sigma^2{}_w + \sigma^2{}_D + ((1+\tau-\alpha).\sigma_{T_{clk}})^2}} \right)$$

Failure for a single SETTOFF:

$$Fr' = g1 \cdot g2'$$

Multiple-SET Failure Rate Model for RF

$$Fr(m) = C_m^n \times Fr^m \times (1 - Fr)^{(n-m)}$$

Where:

n= The number of radiation hits (The number of SETs at the RF input)
m= The number of corrupted bits (number of MBUs)

Note: This equation can derive both the multiple-SET failure rate for a conventional RF, and a SETTOFF-based RF, according the Fr that is chosen.

Comparative Results for RF Failure Rate

Multiple-SET failure rate results for RF. (m=5, TRD interval = 500ps)

	No error	1-bit	2-bit	3-bit	4-bit	5-bit
SETTOFF RF	82%	17%	1.4%	0.06%	0.0012%	$1E^{-5}\%$
ECC/Original RF	5%	21%	34%	28%	11%	18%

Multiple-SEU failure rate results for RF

	1-bit	2-bit	multiple-bit
Original RF	100%	100%	100%
SEC-DED ECC-based RF	0%	Detected	100%
SETTOFF-based RF	0%	0%	0%

SEC-DED: Single Error Correction- Double Error Detection

Comparative Results for Implementation Overhead

- Technology: 65nm
- Frequency: 1GHz
- Supply Voltage: 1.2V

The implementation overhead in 65nm technology

	Area overhead	Power overhead	Delay overhead
SEC-DED ECC-based RF	30%	90%	1 extra cycle
SETTOFF-based RF	70%	44%	13.2%

Notice: The delay overhead of the ECC-protected RF is big due to the large decoding block at the read port, therefore an extra cycle may be required to reload the register for error correction.

Conclusion

- The SETTOFF-based RF can efficiently tolerate both SETs and SEUs. ----- The combinational logic occupies the majority of the cell area in RF, but ECC can not address SETs.

- The MBUs induced by multiple-SETs and multiple-SEUs can also be tolerated. ----- ECC requires a noticeable larger overhead to address MBUs

- On-the-fly correction of SEUs

- Significant power saving (50%) over ECC

- Significant less delay overhead than ECC.

- The area overhead is acceptable ----- less than DMR.