StatDes

Variation is the Future

March 17th 2014

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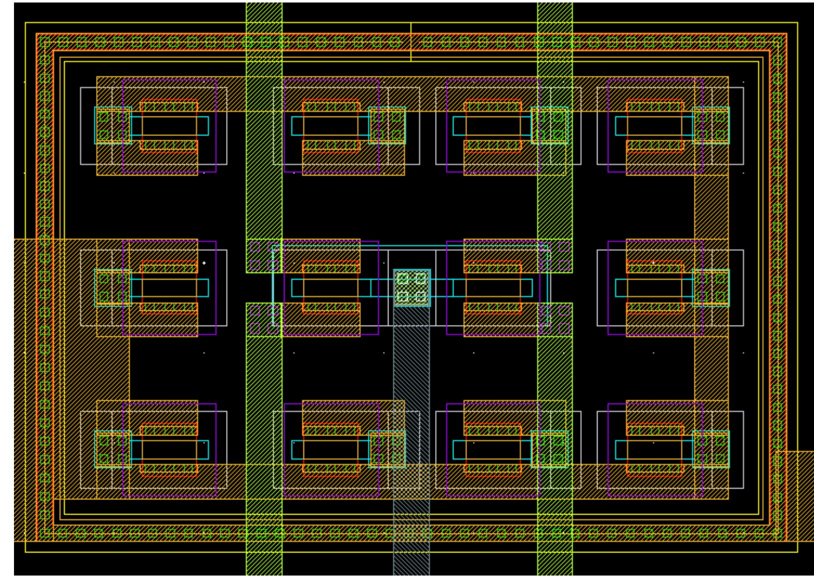
Variation in Deep-Submicron CMOS

- Industry pressures continue to shrink process nodes
  - Consumer desires smarter, lower-power devices
- Technologies are optimised for the majority (digital) devices
  - Analogue/Mixed-Signal still crucial for functioning Systems-on-Chip
- Active device area is now reaching a point where the discrete nature of charge and matter are noticeably impacting device performance.
- Key processing steps are stochastic
  - intrinsic variation in device performance
  - overwhelms the contributions of process gradients (small-to-medium devices)
- Correct understanding of variability is essential
  - identify problematic circuit elements
  - reduce overdesign of circuit blocks where there is no benefit.

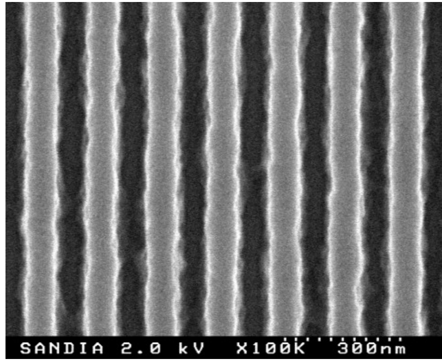
Traditional Analogue Solution

- Methodology: spend area to mitigate variation
  - ➢ Increasingly costly with each node shrink
- Careful layout -> good matching
  - ➢ Consistency of environment
  - ➢ Symmetry
  - ➢ Inter-digitation
  - ➢ Dummy structures
- Layout reduces systematic mismatch
- Active area reduces intrinsic mismatch
- Opportunities for alternatives available (system-level solutions)
  - ➢ Digital sections are cheap
  - ➢ Calibration, reconfiguration and post-processing (digitally assisted analogue).



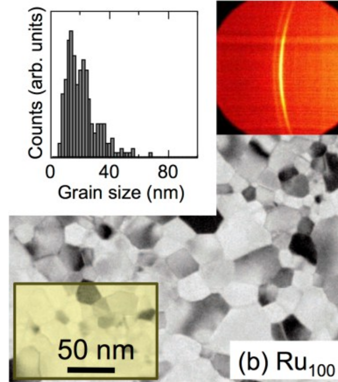
Symmetrical differential-pair layout with a ring of dummy devices.

Intrinsic Variation Sources



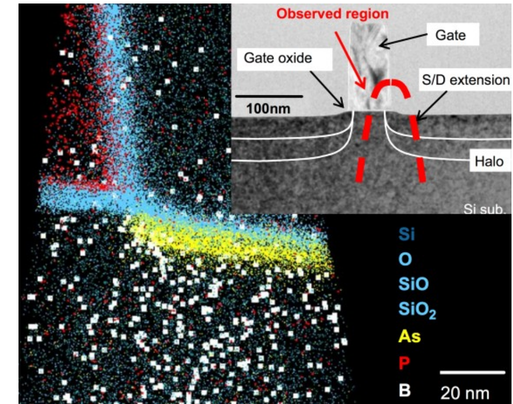
SANDIA Labs

Line Edge Roughness (LER)



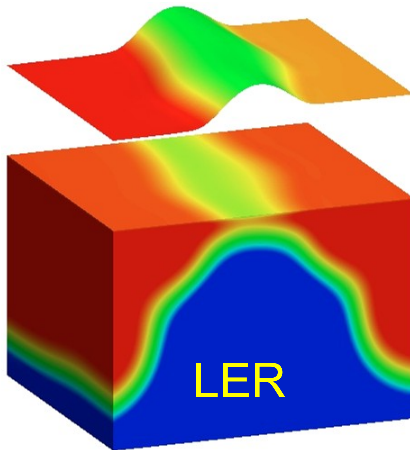
Ohmori, IEDM'08

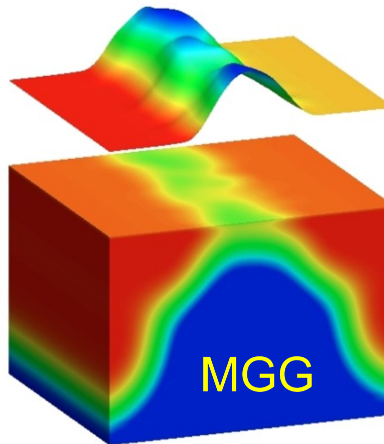
Metal Gate Granularity (MGG)

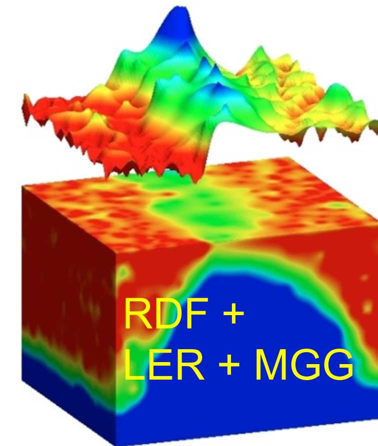


Inoue '09

Random Dopant Fluctuation (RDF)







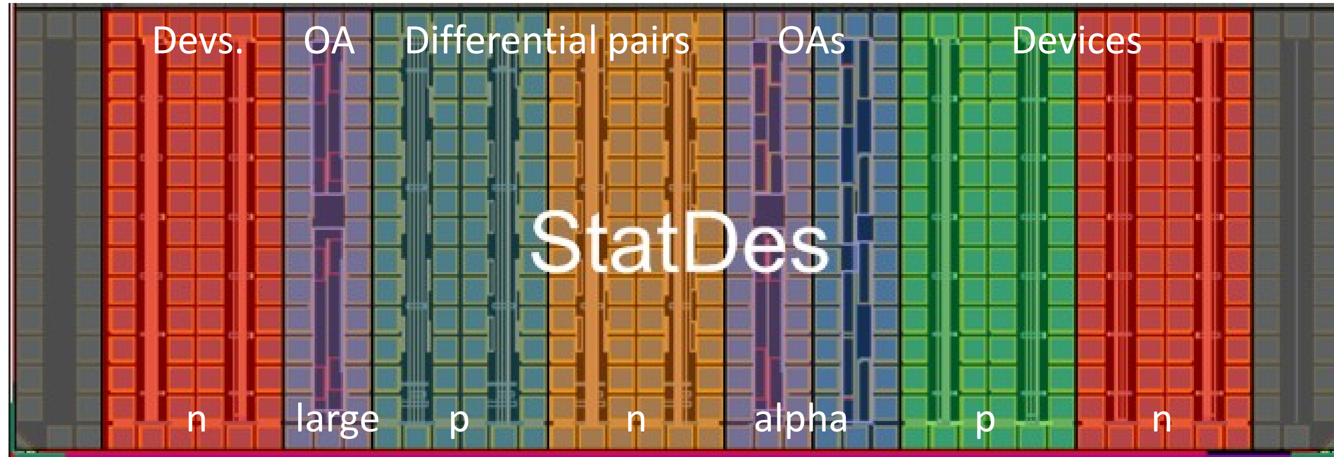
Atomistic device simulation can help quantify the impact on device performance.

StatDes

- A collaborative project between academia and industry to investigate intrinsic variability of deep-submicron devices for analogue circuits.
- Primary goal is to verify the compact model extraction and statistical simulation tools developed by academia and show how they can be used to augment the existing tool-chains in use by industry.

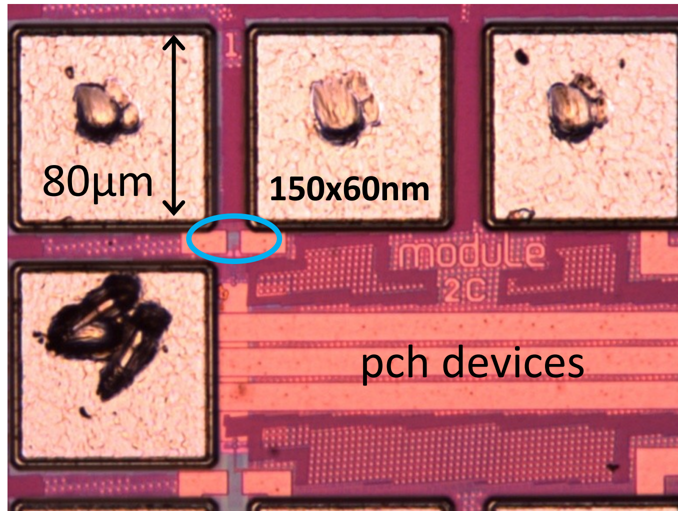
- Phase One: Test Chip Design and Fabrication (65nm bulk CMOS)
- Phase Two: Measurement and Compact Model Extraction
- Phase Three: Verification and Statistical Simulation (Current Work)

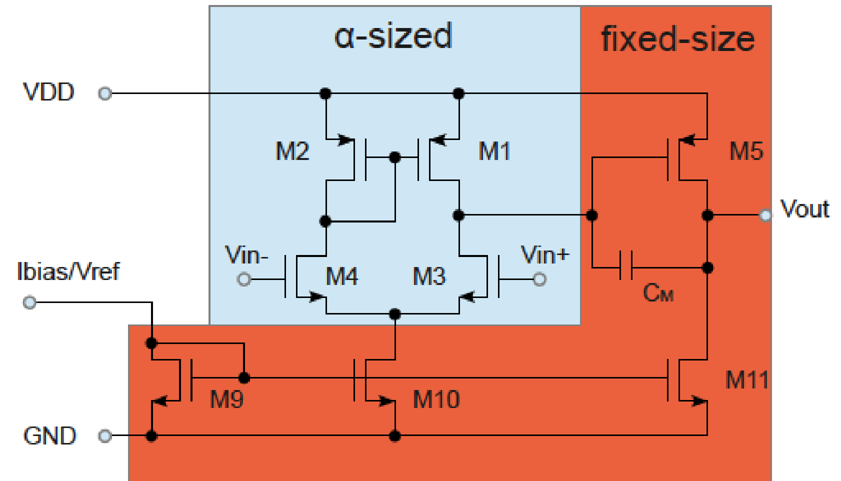
Fabricated Test Chip



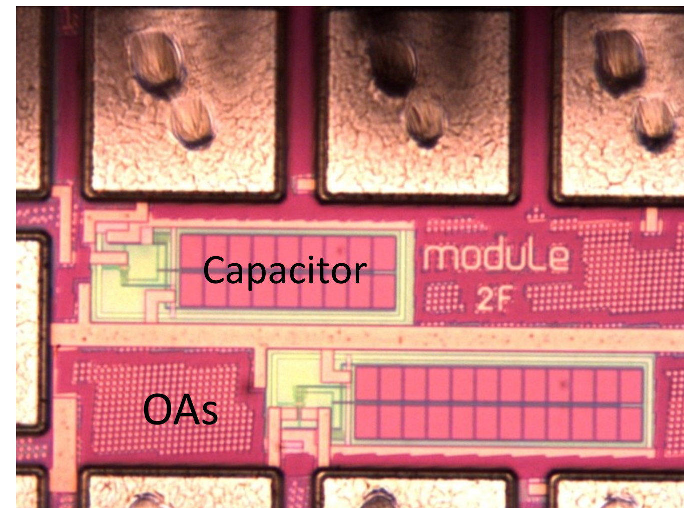
- Common 32-pad ring structure used for all modules
- 13 modules of devices, differential-pairs and basic Operational Amplifiers:
  - Devices: 14 per module (common bulk and gate connections)
  - Diff-pairs: 7 pairs per module (common bulk and gate connections)
  - Op-Amps: 8 per module (two-stage, Miller compensated)
- 78 instances of the test chip were available for measurement using probe-stations at Glasgow and Edinburgh Universities.

Fabricated Test Chip

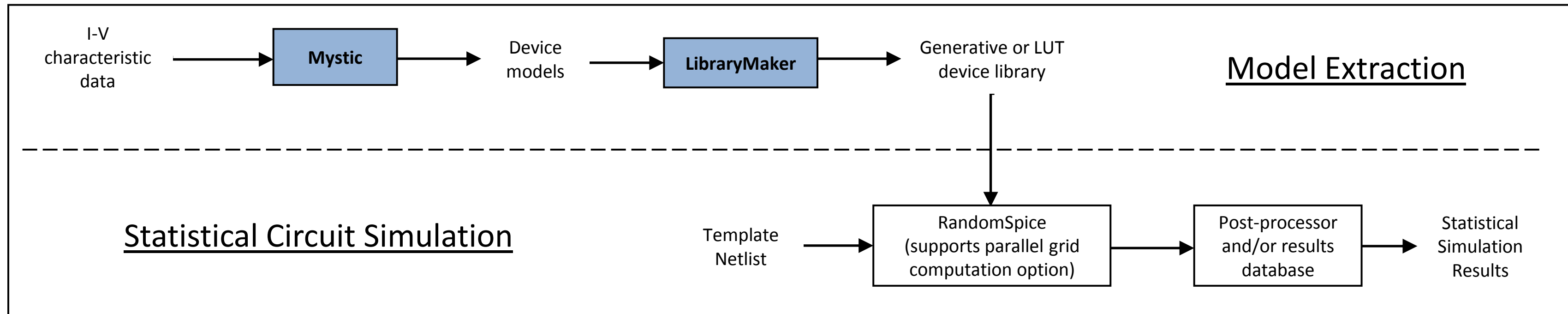




- Individual device characterisation is very area intensive
- More informative structures:
  - Individual gate connections
  - Repeated differential-pairs (closer proximity) rather than more dimensions



Compact Model Extraction

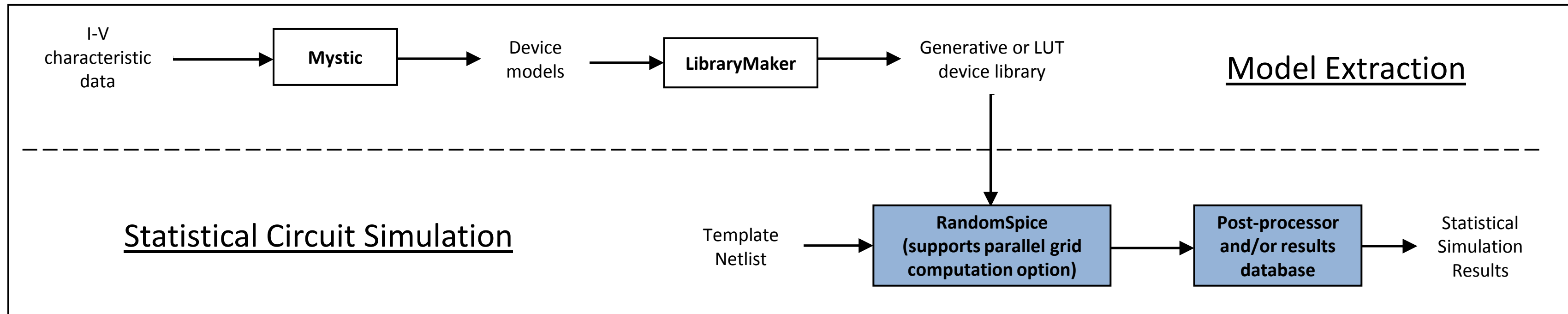


- GSS Mystic: I-V characteristics -> compact models
  - Initial nominal extraction requires manual intervention (selection/tuning)
  - Subsequent fitting of statistical parameters is automated and quick
- Constructed device libraries:
  - Device Look-up Tables (LUTs)
  - Generative models (derived from parameter distributions)
- In this work compact models extracted from device measurements
  - Alternatively this data could be obtained through atomistic simulation
  - Individual variation sources
  - Technologies not yet in production

Compact Model Extraction

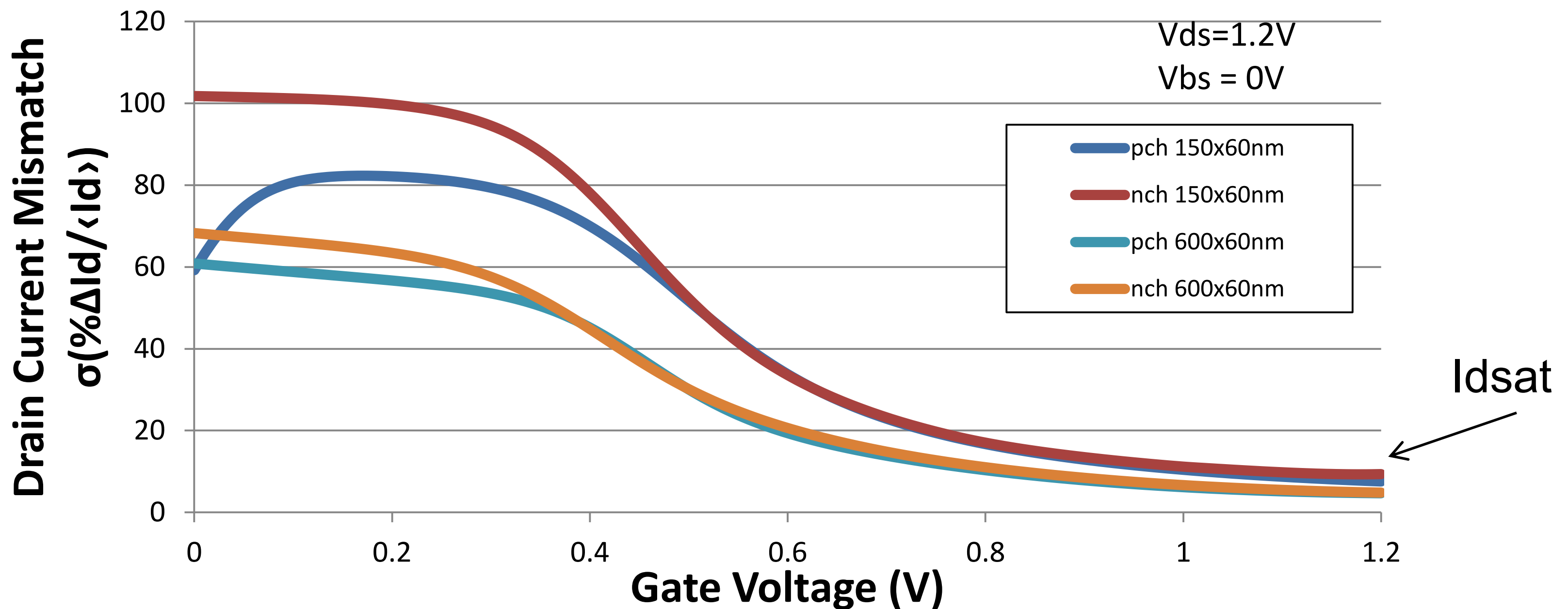
The result is fitted models accurate across the full operating range of the device.

Statistical Simulation



- GSS RandomSpice:
  - Template netlist driven work-flow (library specific model keywords)
  - Creates specific netlist instances from LUT or generative models
  - Simulation performed sequentially or submitted to a compute grid
- Data management support:
  - Potential for vast numbers of data
  - User-scripted post-processing modules
  - Backend database storage

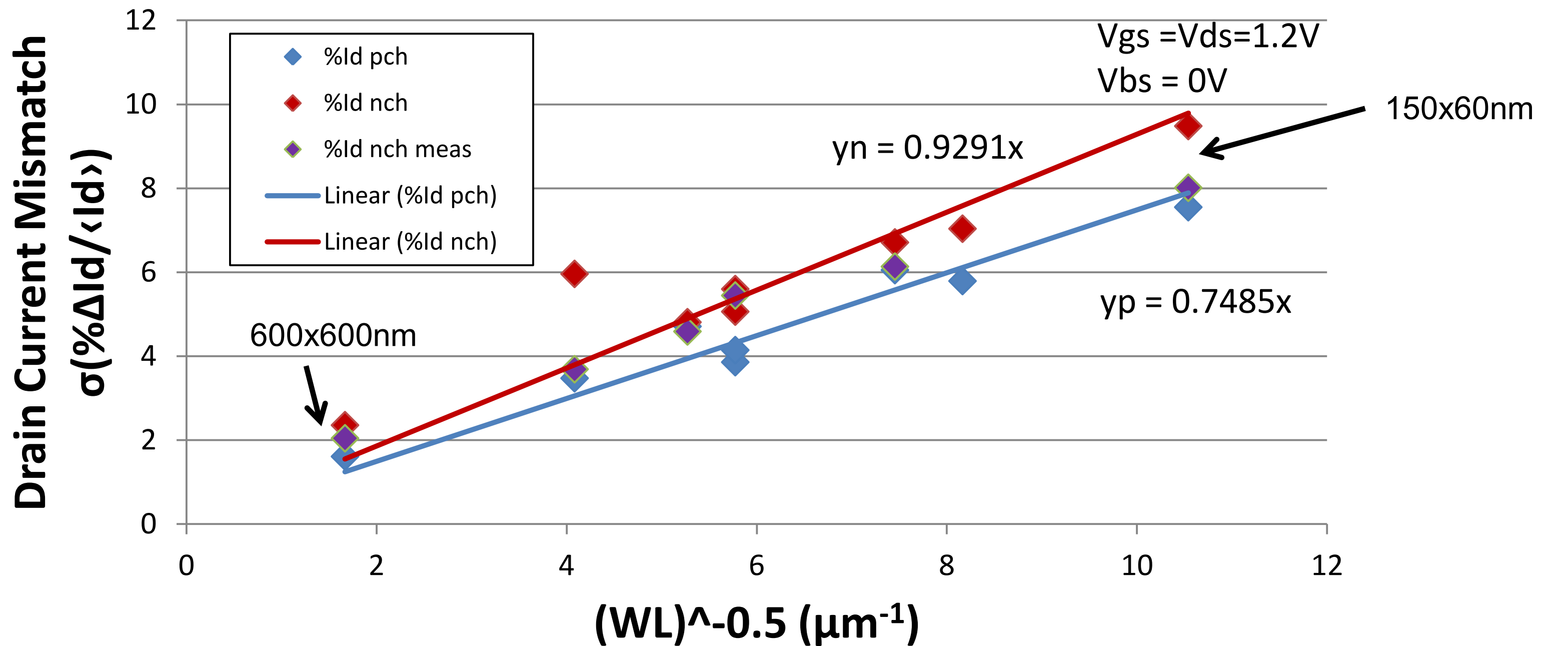
Local Mismatch Plots [Tuinhout CICC13]



Local mismatch variation plot of drain current against gate voltage for small geometry devices in saturation extracted from differential pair measurements.

Useful tool for investigating the impact of parametric gradients on device matching. Tuinhout et al have found that careful attention to the layout is more important for matching than keeping a short distance between the components.

Pelgrom Area Scaling



Pelgrom plot of drain current mismatch for eight device geometries. Area scaling continues to be applicable with a slightly better per area matching of pch devices.

The Future?

- Current CAD/EDA tools generally support the use of statistical models and simulation of circuit designs to verify their behaviour.
- This provides necessary confidence that a circuit block will yield correctly when manufactured
- However, on its own this does not provide insight into what elements are sensitive to variation or should be modified to reduce overdesign.
- Tools should further support statistical analysis and data mining of simulation results
  - augment designer expertise
  - allow for a rapid exploration of the design space
  - ensure variation-awareness from the initial nominal design.

Questions?