Automatic MOSFET Sizing to Maximize the Lifetime Yield of Analog Circuits

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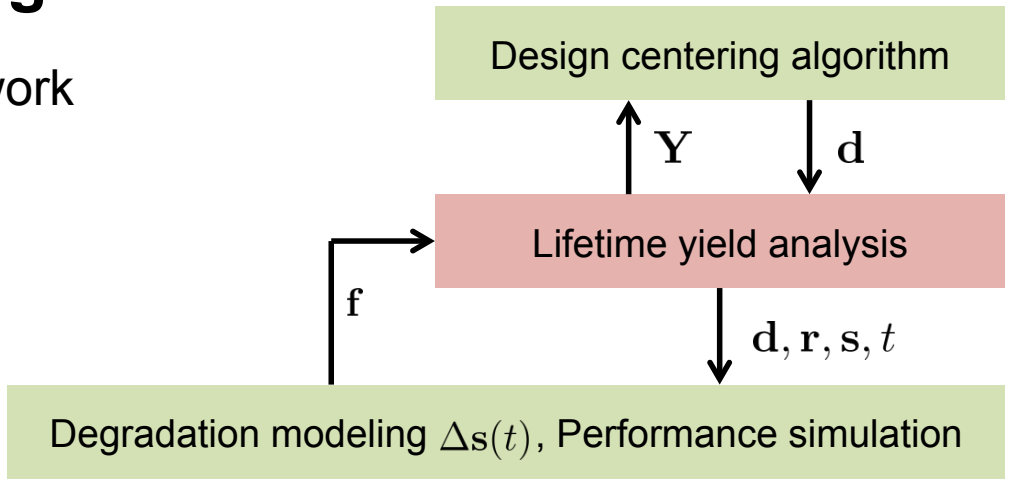
Contents

Overview of circuit sizing

Components of the design framework

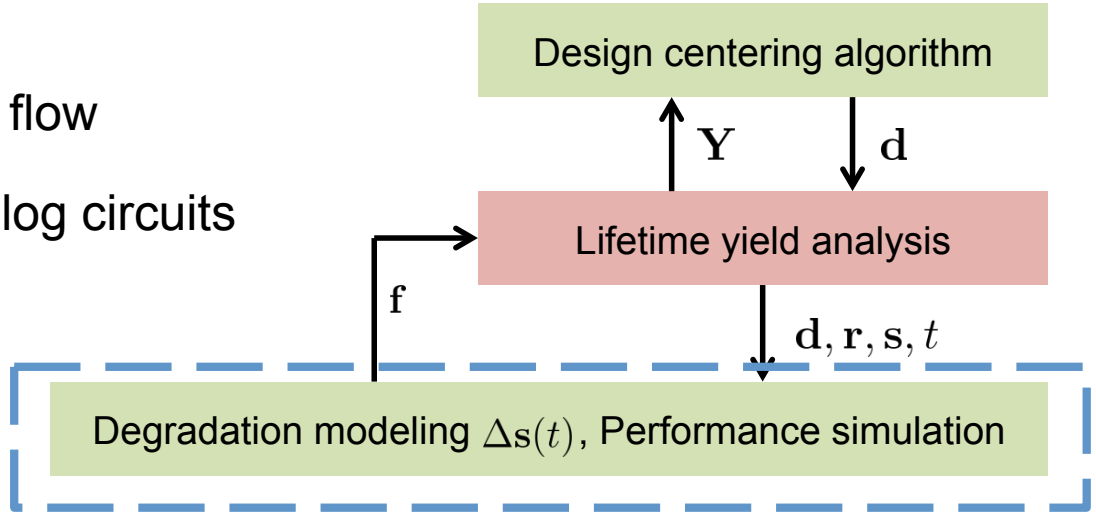
- Design centering
- Lifetime yield analysis
- Performance simulation
- Degradation modeling



Design parameters	$\mathbf{d}$	MOSFET width (W), length (L)
Operating parameters	$\mathbf{r}$	Temperature (T), Supply (Vdd)
Statistical process parameters	$\mathbf{s}$	Threshold voltage (Vth), Toxe
Operating time	t	Hours, days, years
Parameter degradation	$\Delta\mathbf{s}$	$\Delta\mathrm{Vth},\ \Delta\mathrm{Id}$
Performances	$\mathbf{f}$	slew rate, gain, power
Parametric yield	$\mathbf{Y} = \mathrm{Prob}\left\{\mathbf{f}_l \preceq \mathbf{f}\right\}$	

Contents

- Overview of the circuit sizing flow
- Degradation modeling in analog circuits
  - Problems and workarounds
  - Circuit example
- Lifetime yield analysis
- Constrained design centering
  - Circuit example
- Conclusion



Degradation modeling

- MOSFET degradation mechanisms, such as BTI and CHC
- Change in MOSFET attributes
- BTI model [da Silva 2010, Gasser 2011, Barke 2013/4]
  - Temperature (T) and Fermi-level dependency (~Vgs)

$$A\left(T, \mathrm{Vgs}\right) = K \exp\left(-\frac{E_0}{k_B \cdot T}\right) \exp\left(\frac{-B \cdot \mathrm{Vgs}}{\mathrm{Toxe} \cdot k_B \cdot T}\right)$$

  - Electric field, E, applied

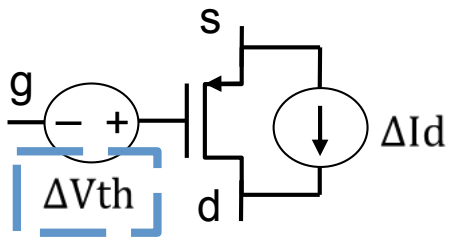
$$\Delta\mathrm{Vth}\left(t\right) \propto A\left(T, \mathrm{Vgs}\right) \cdot \sum_{i=1}^{2} \alpha_i \cdot log\left(1 + t/\tau_{c,i}\right); \quad \tau_{c,1} = 1\,\mathrm{ms}, \tau_{c,2} = 1\,\mathrm{ks}$$

  - Recovery period, E⟶0

$$\Delta\mathrm{Vth}\left(t\right) \propto -A\left(T, 0\right) \cdot \sum_{i=1}^{2} \beta_i \cdot log\left(1 + t/\tau_{e,i}\right); \quad \tau_{e,1} = 20\,\mu\mathrm{s}, \tau_{e,2} = 1\,\mathrm{Ms}$$

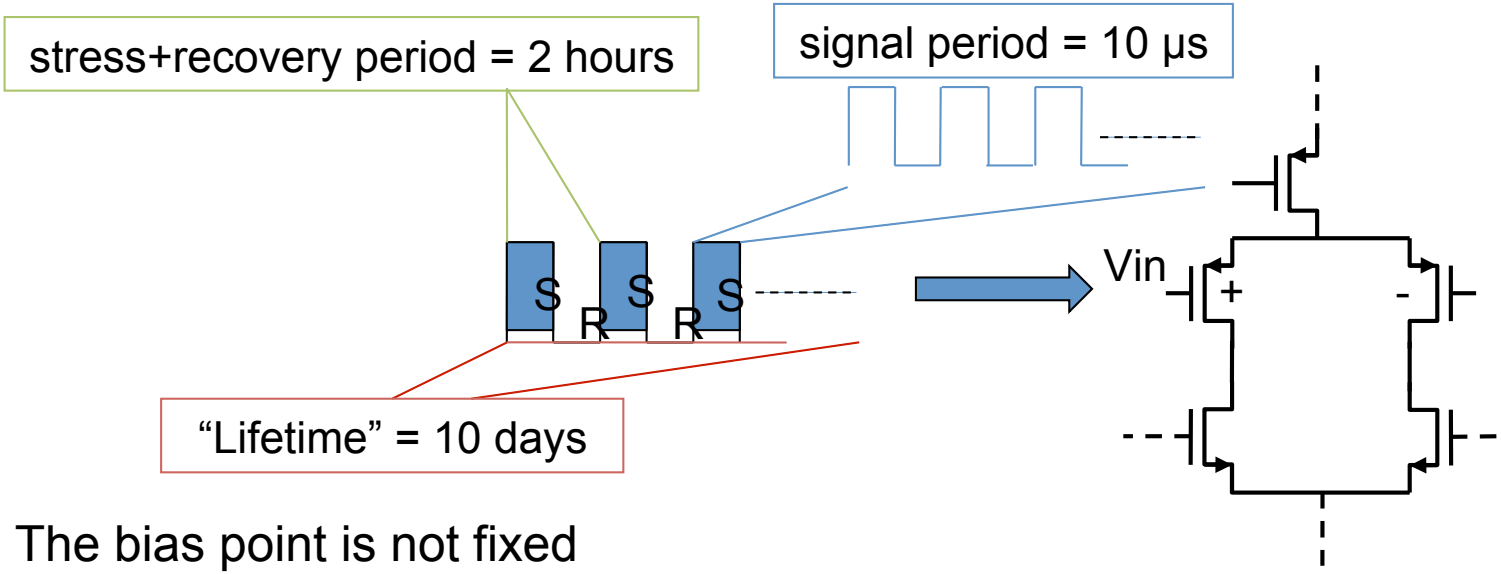
  - Variance [Grasser 2013]

$$\sigma^2\left(\Delta\mathrm{Vth}\right) \propto \frac{\mathrm{Toxe} \cdot \Delta\mathrm{Vth}}{W \cdot L}$$



Degradation modeling – analog implementation

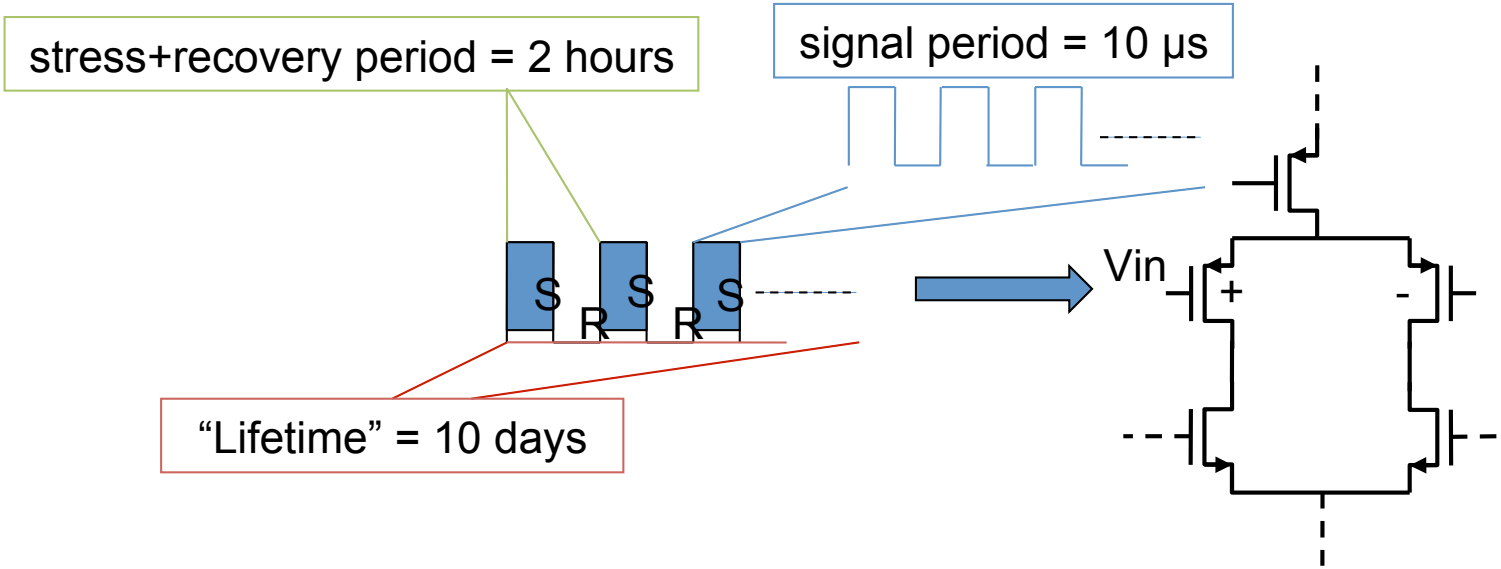
- Differential input stage with cyclostationary analog input



- Problem: The bias point is not fixed
  - $\mathbf{v}(t+dt) \leftarrow \phi(t, \mathbf{v}(t), Vin(t), \Delta\mathbf{s}(t))\,; \;\; \mathrm{Vgs}(t) = \mathbf{M}^T \cdot \mathbf{v}(t)$
  - $\mathbf{v}(t)$ are the node voltages, $\phi(\cdot)$ is the circuit state equation, $\mathbf{M}$ is an incidence matrix
  - $Vin(t)$ is periodic with a signal period $\tau_{\mathrm{sig}} = 10\,\mu\mathrm{s}$
  - $\Delta\mathbf{s} = [\Delta\mathrm{Vth}_1(t), \Delta\mathrm{Vth}_2(t), \ldots]$ the vector of change in all circuit devices

Degradation modeling – analog implementation

- Differential input stage with cyclostationary analog input



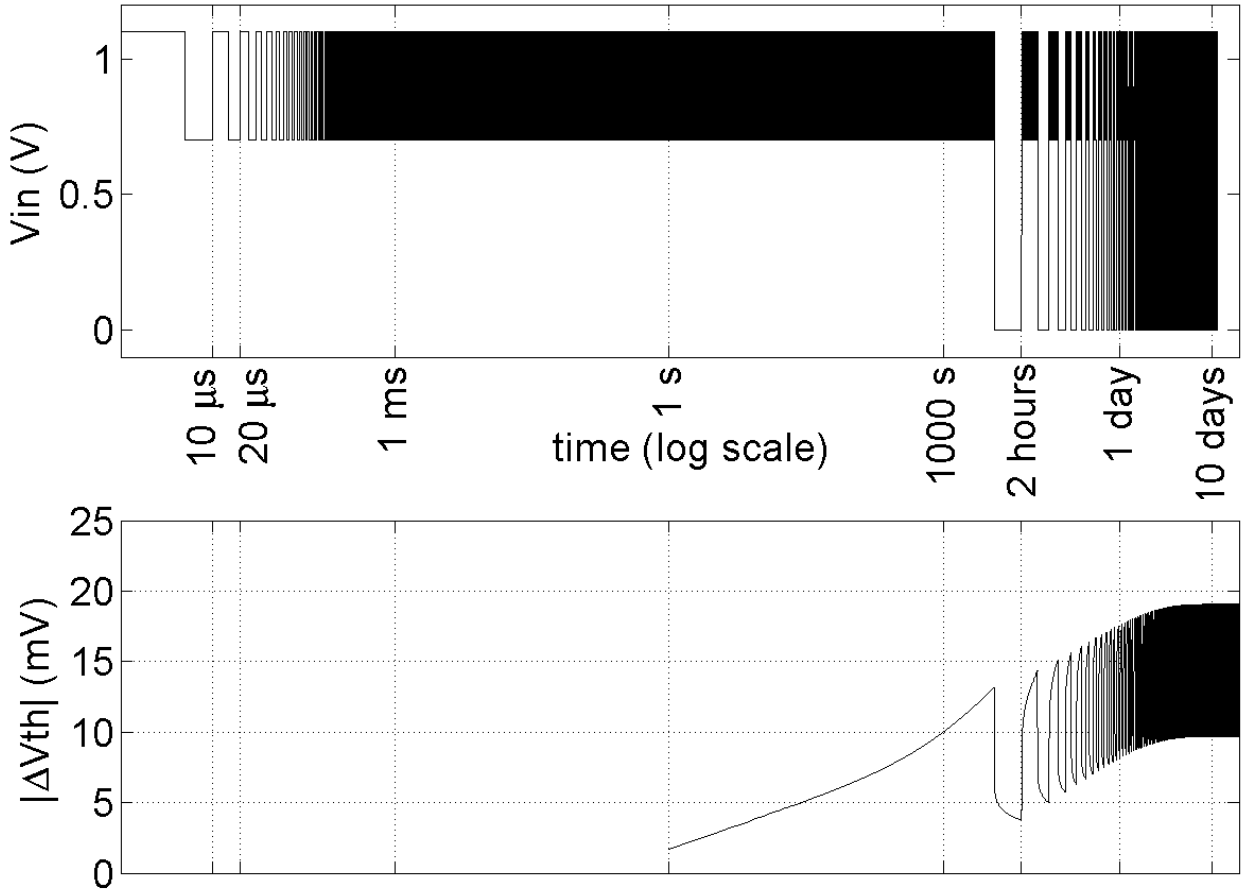
- Solution:
  - At small timescales when $\tau_{\mathrm{sig}} \ll \tau_{c,1}$, $\Delta\mathrm{Vth}(t+\tau_{\mathrm{sig}}) \approx \Delta\mathrm{Vth}(t)$ (fixed)
  - Average the Fermi-level dependency over the input period

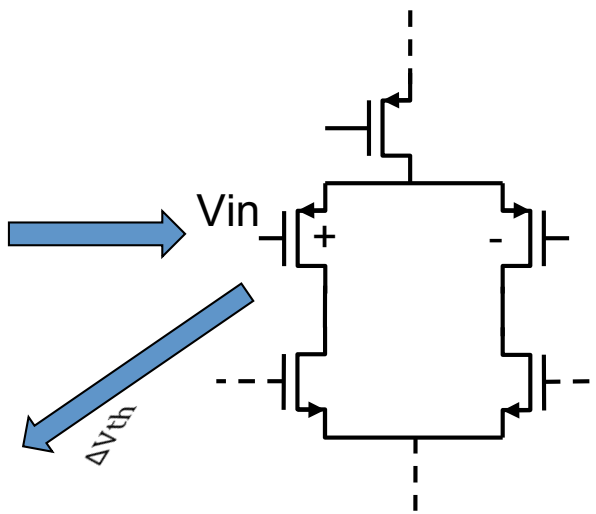
$$\bar{A}\left(T, \tilde{\mathrm{V}}\mathrm{gs}\right) \longleftarrow \frac{1}{\tau_{\mathrm{sig}}} \int_{\tau=t}^{\tau=t+\tau_{\mathrm{sig}}} A\left(T, \mathrm{Vgs}\left(\tau\right)\right) d\tau$$

  - Recalculate $\bar{A}\left(T, \tilde{\mathrm{V}}\mathrm{gs}\right)$ at large time steps to accommodate changes in $\Delta\mathrm{s}$
  - Computational cost: a transient simulation for each recalculation

Degradation modeling – analog implementation

- Differential input stage with realistic cyclostationary analog input

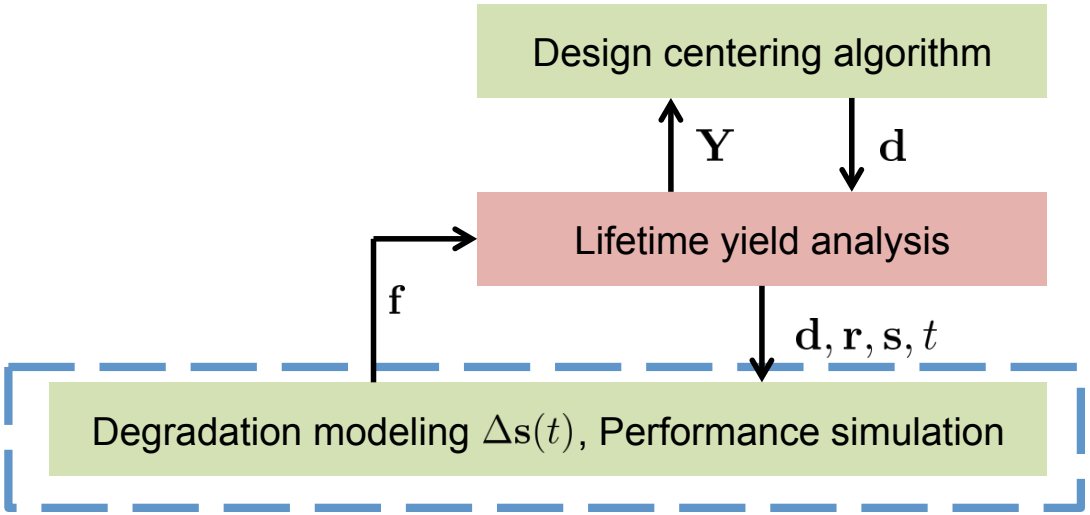




Cost: 5 transient simulations

Degradation modeling – performance simulation

- Simulate the effect of degradation on circuit performances $\mathbf{f}$
  - t_{sim} is the duration needed for calculation of $\mathbf{f}$
  - Performance simulation: $\mathbf{v}\left(t+dt\right) \leftarrow \phi\left(t, \mathbf{v}\left(t\right), Vin\left(t\right), \Delta\mathbf{s}(t)\right); \;\; \mathbf{v}(\tau)_{\tau=t}^{\tau=t_{\mathrm{sim}}} \mapsto \mathbf{f}$



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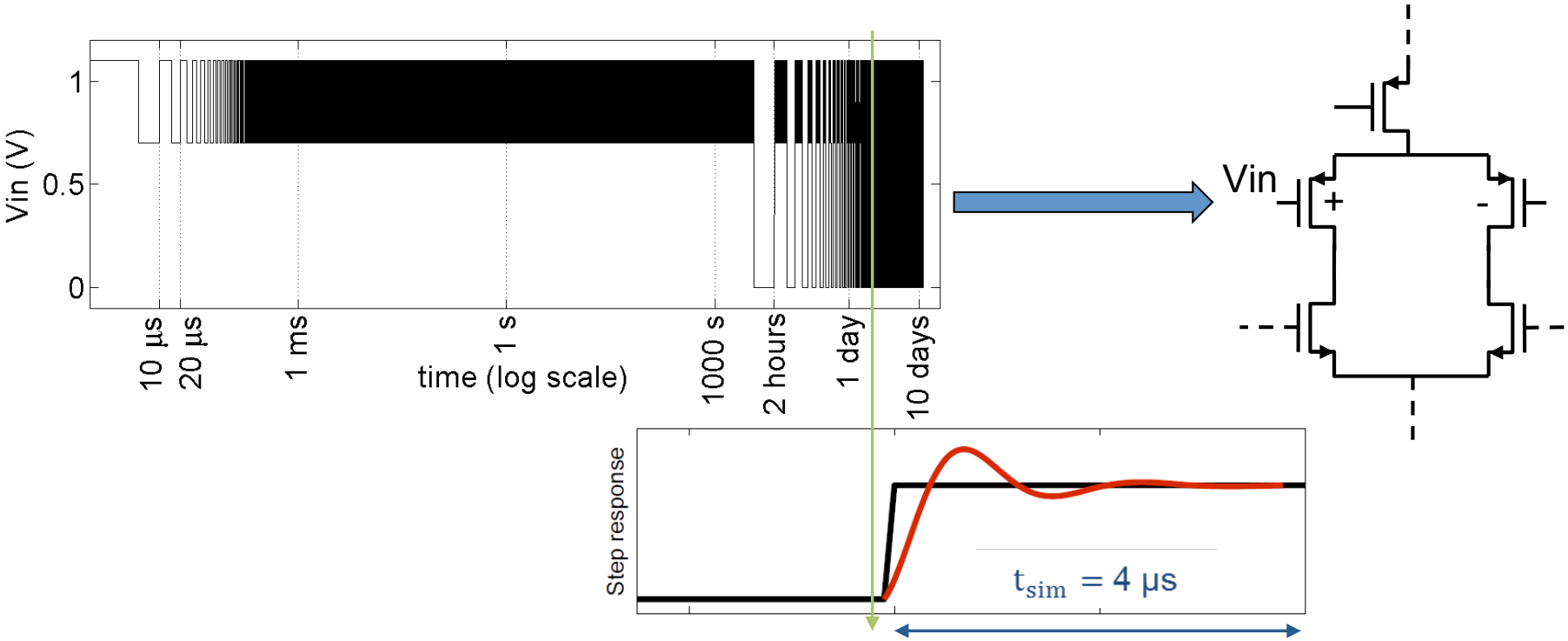
- Example: simulate step response to calculate settling time



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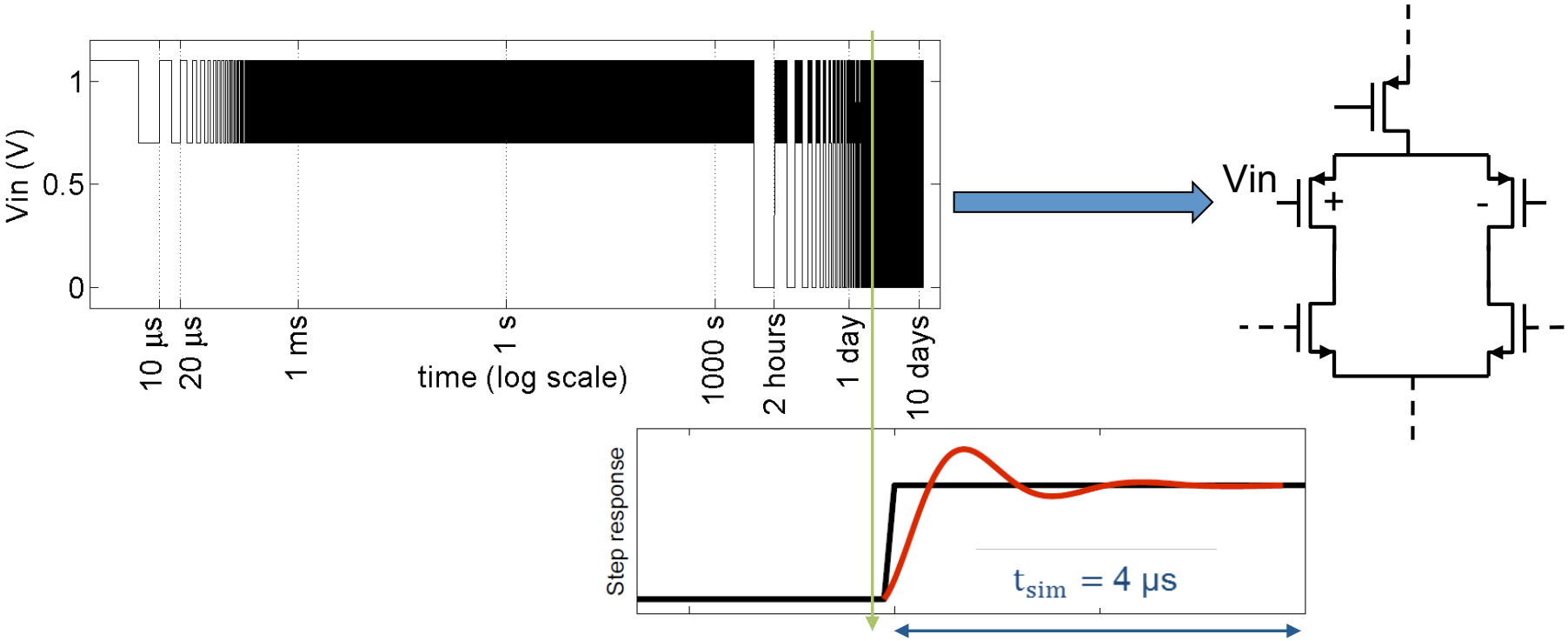
- Problem: need to model degradation *during* performance simulation (t_{sim})



Degradation modeling – performance simulation

- Simulate the effect of degradation on circuit performances $\mathbf{f}$
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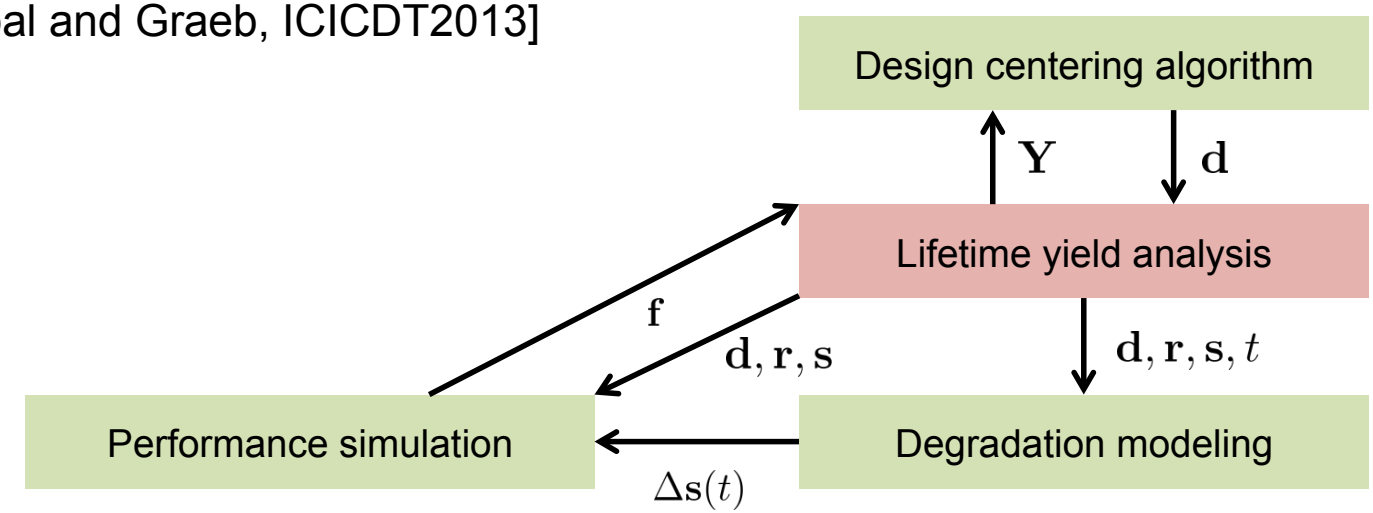
- Problem: need to model degradation *during* performance simulation (t_{sim})
- Solution: if $t_{\mathrm{sim}} \ll \tau_{c,1}$, then $\Delta\mathbf{s}(t+t_{\mathrm{sim}}) \approx \Delta\mathbf{s}(t)$;
  $\mathbf{v}\left(t+dt\right) \leftarrow \phi\left(t, \mathbf{v}\left(t\right), Vin\left(t\right), \Delta\mathbf{s}(t) = const\right); \;\; \mathbf{v}(\tau)_{\tau=t}^{\tau=t_{\mathrm{sim}}} \mapsto \mathbf{f}$; the flow becomes
- [Habal and Graeb, ICICDT2013]



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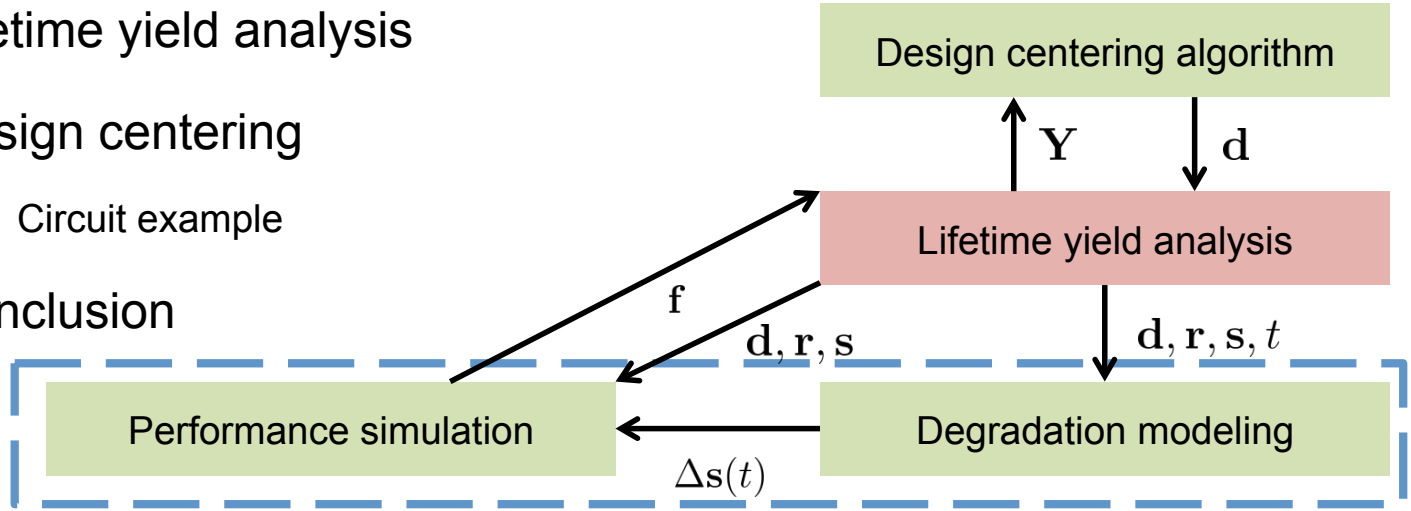
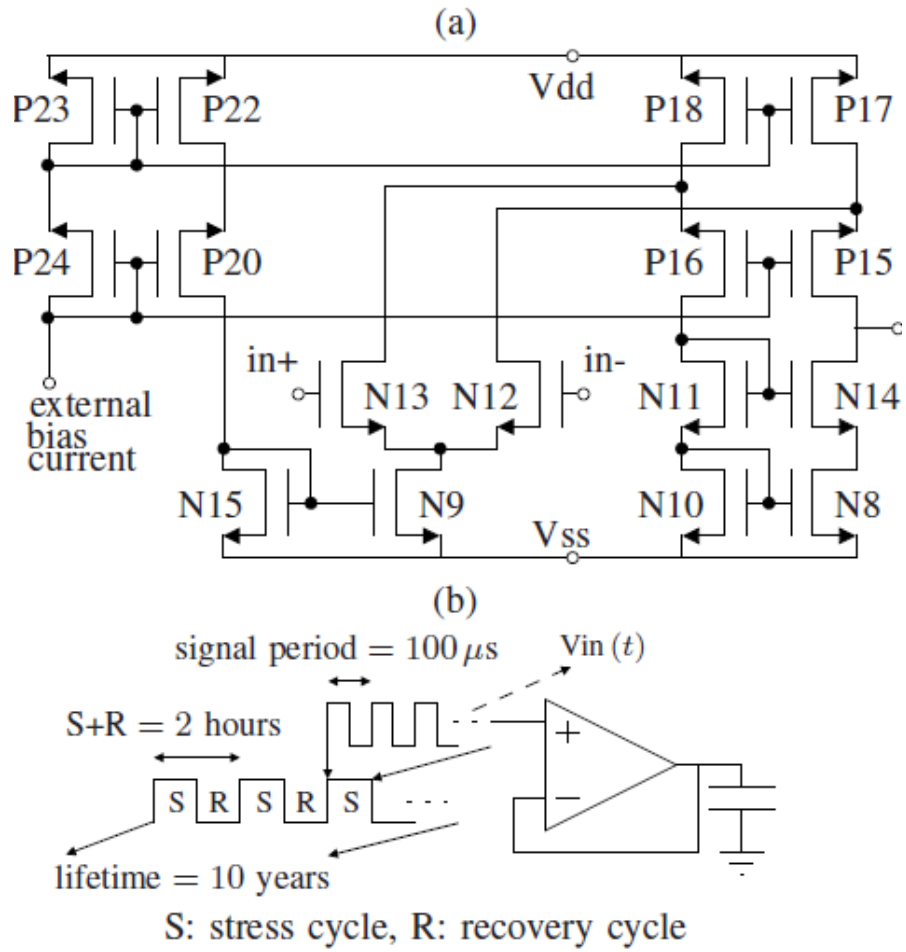


Circuit example

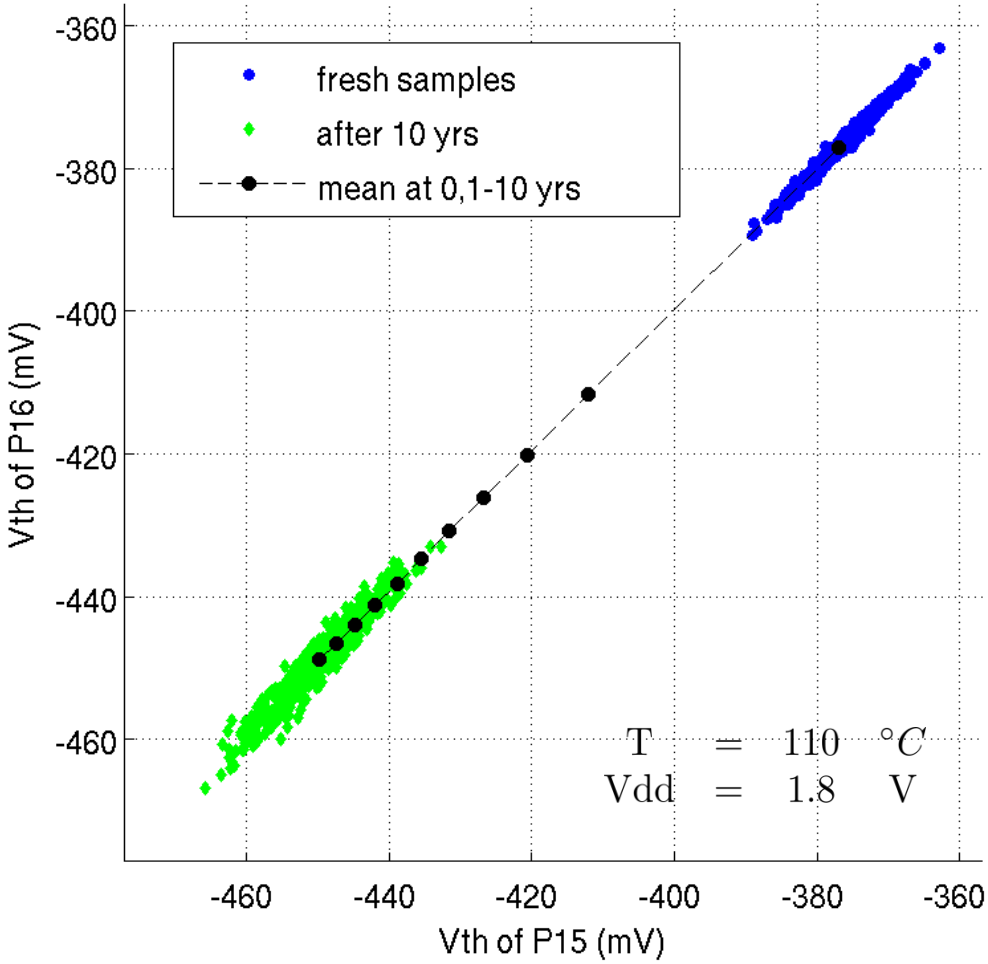
- 45 nm tech [pdk.cadence.com]
- 39 process parameters
- 33 design parameters
- NBTI and HCI modeled
- Operating parameter ranges

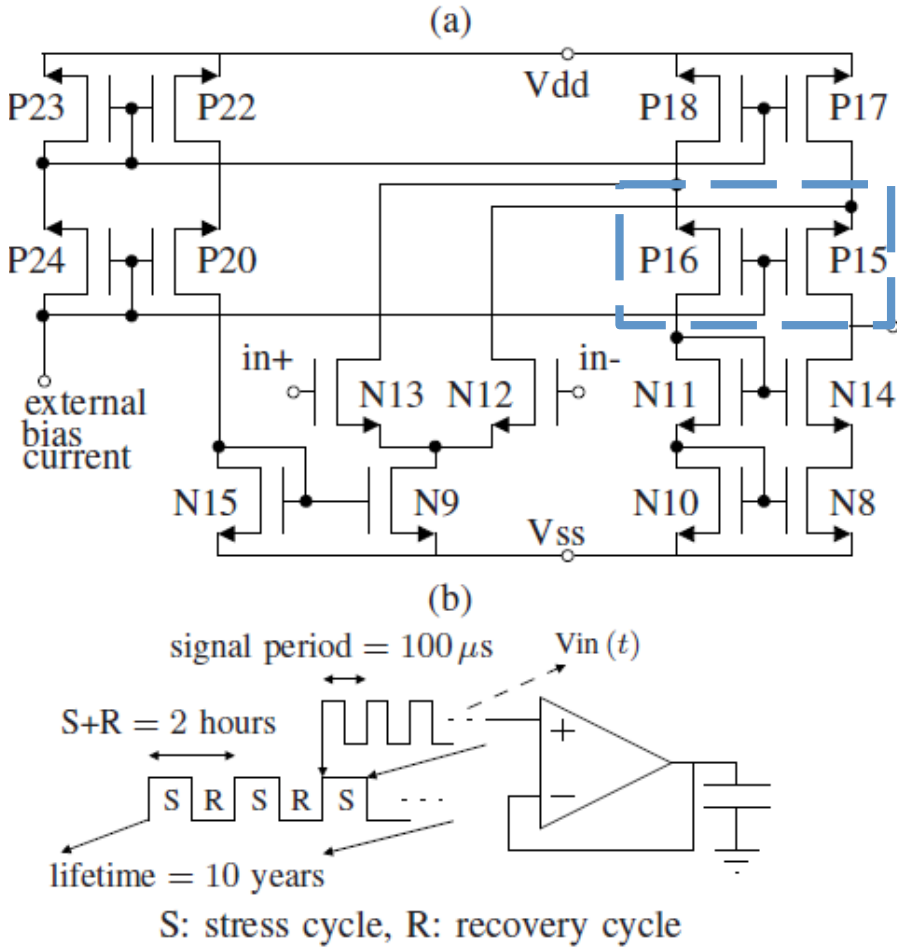
$$\begin{array}{ccccc} 0 & \leq & \mathrm{T} & \leq & 110 \quad {}^{\circ}C \\ 1.8 & \leq & \mathrm{Vdd} & \leq & 2.2 \quad \mathrm{V} \\ 0 & \leq & \mathrm{mag}\{\mathrm{Vin}\} & \leq & 0.4 \quad \mathrm{V} \end{array}$$

- Sized without considering degradation

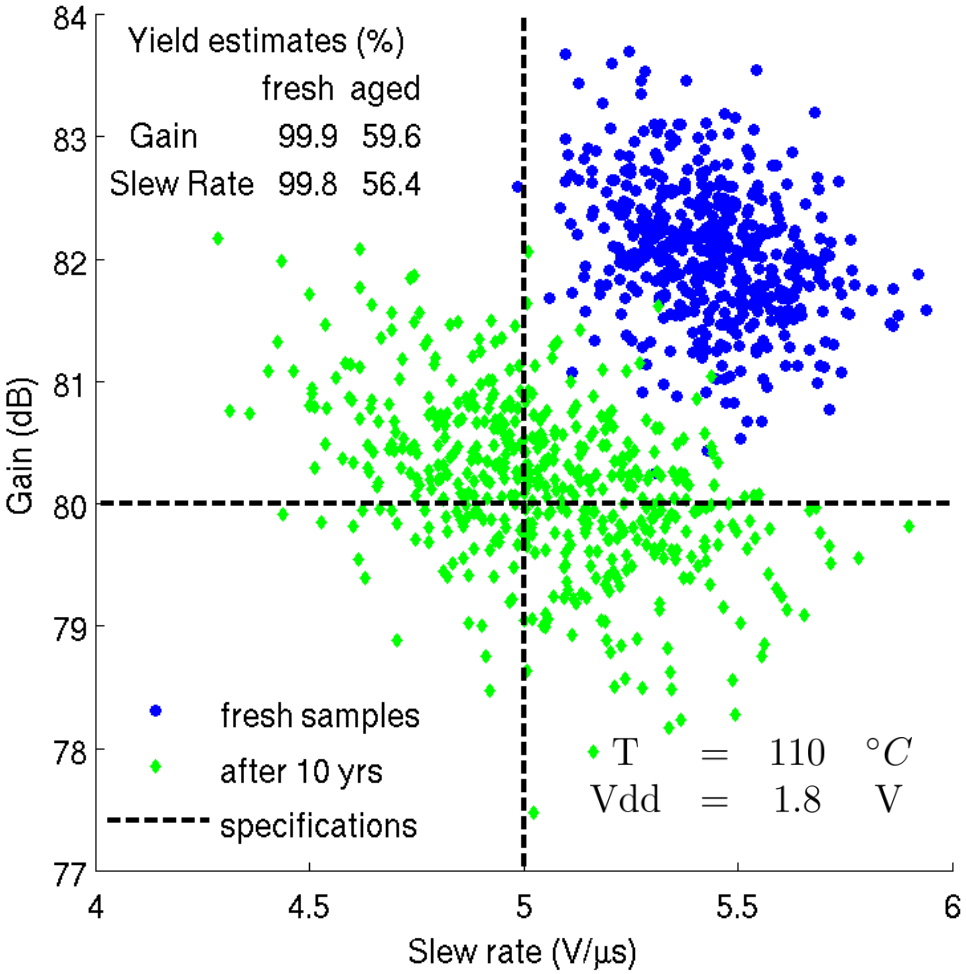


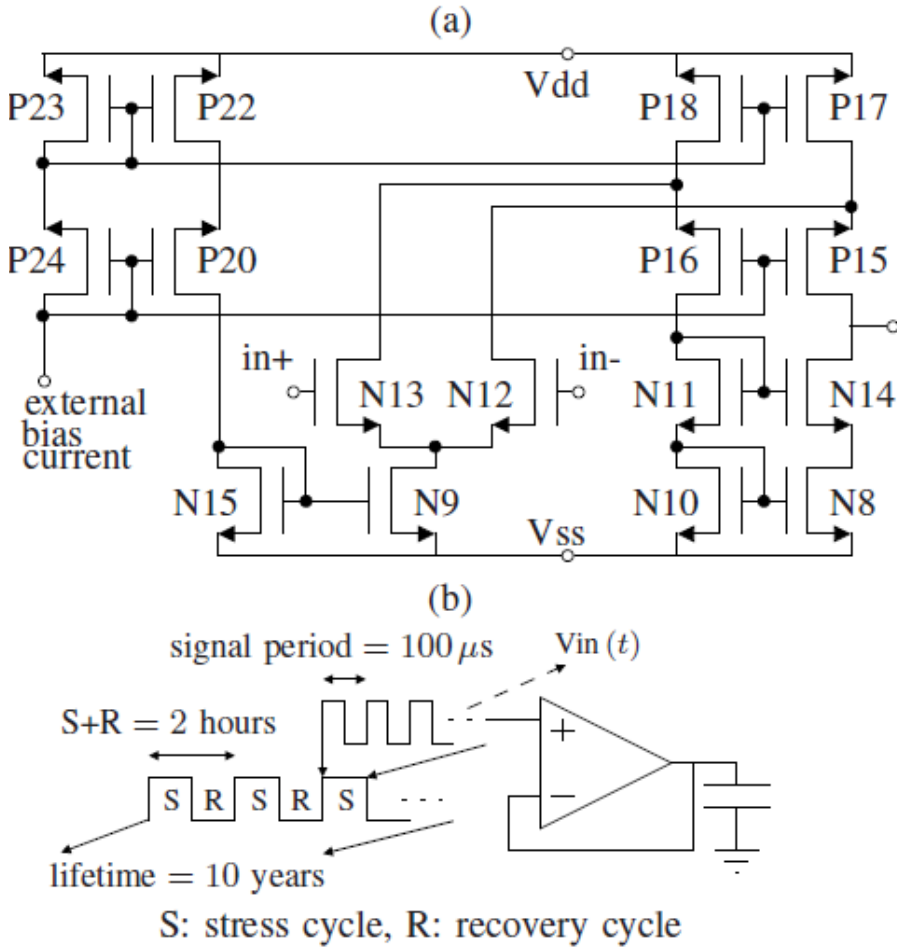
Circuit example





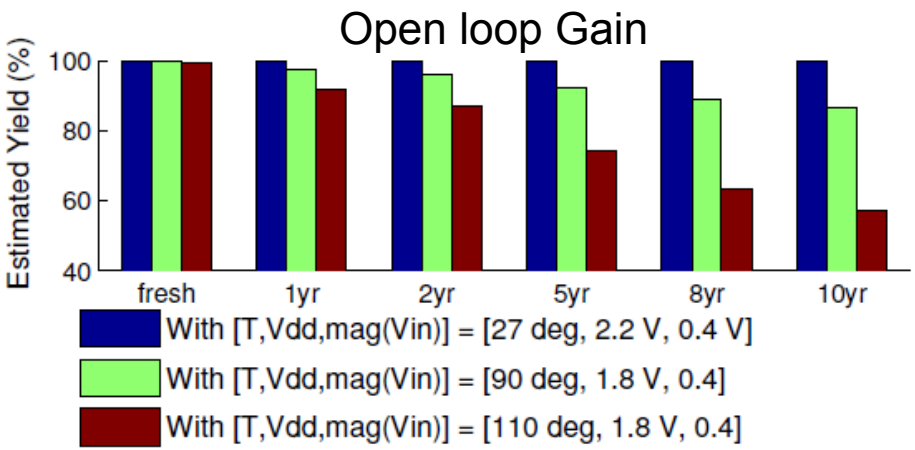
Circuit example

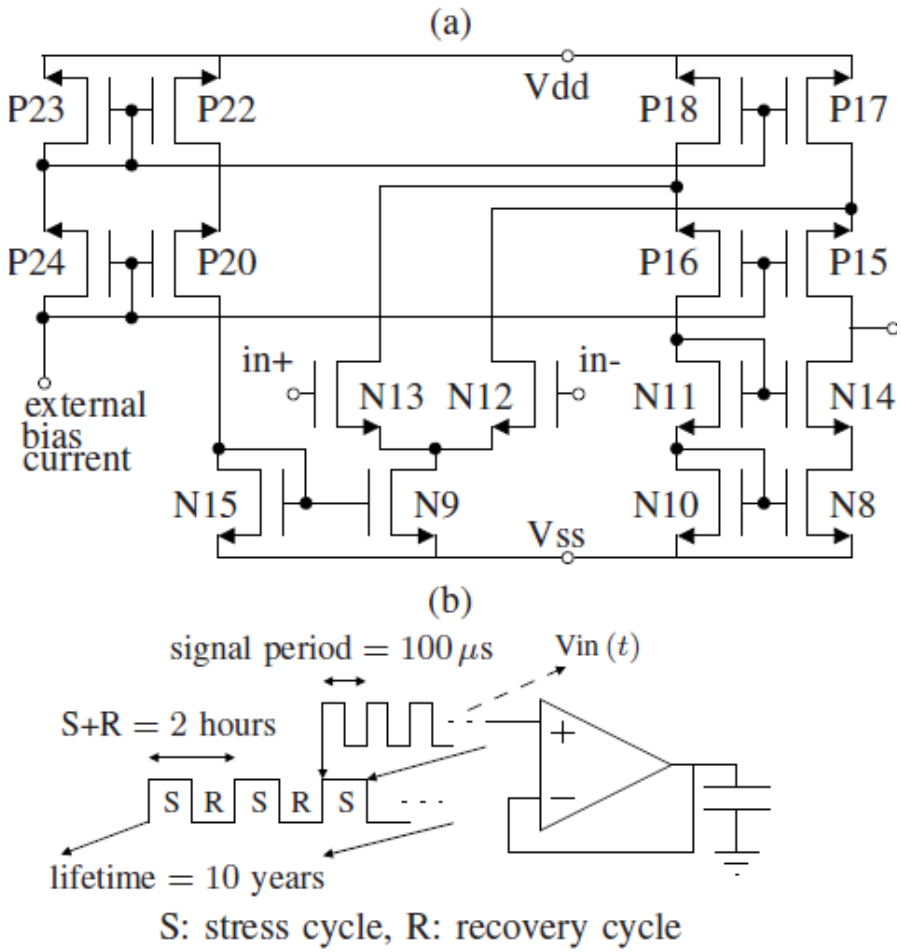




Circuit example

- Operating parameter dependency
  - $$\begin{array}{rcccl} 0 & \leq & \mathrm{T} & \leq & 110 \quad {}^{\circ}C \\ 1.8 & \leq & \mathrm{Vdd} & \leq & 2.2 \quad \mathrm{V} \\ 0 & \leq & \mathrm{mag}\{\mathrm{Vin}\} & \leq & 0.4 \quad \mathrm{V} \end{array}$$
  - Need to consider the worst-case operating corner for degradation:





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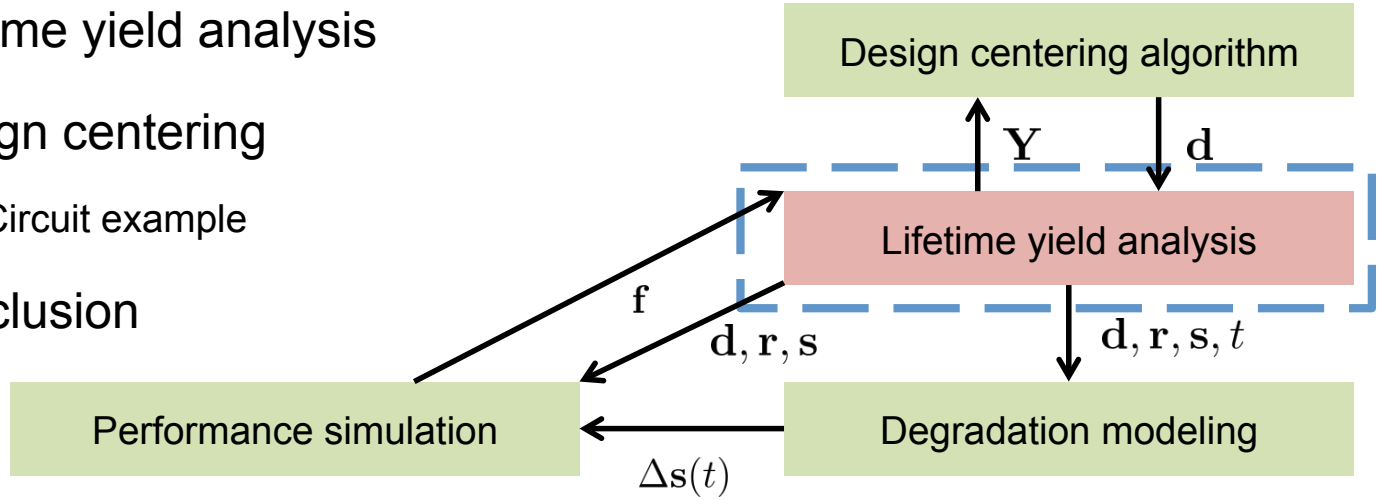
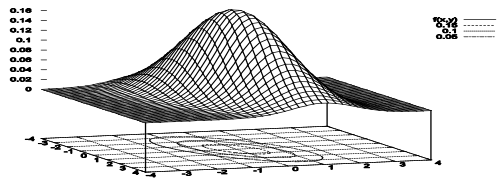
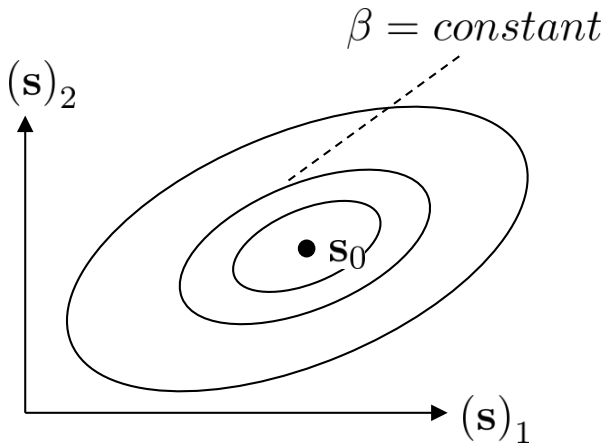


Fresh yield analysis [Graeb 2007]



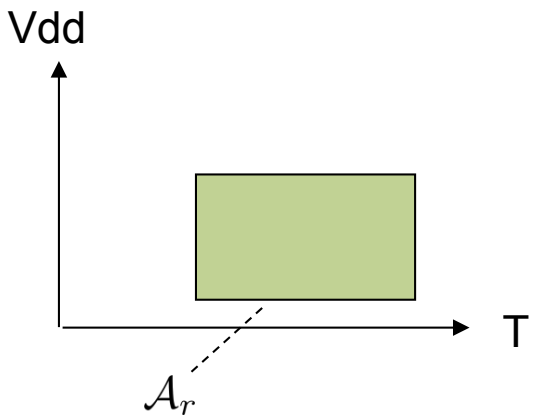


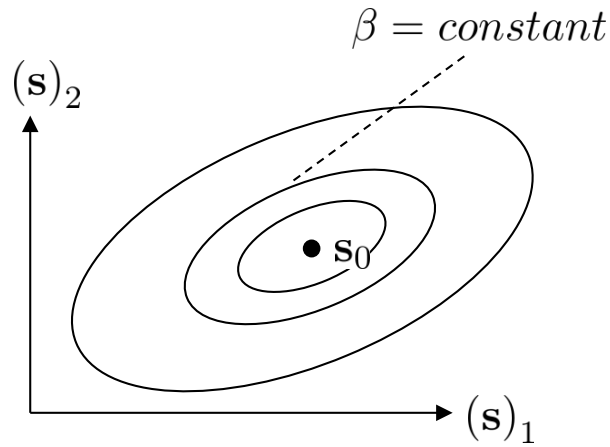
$$\mathrm{pdf}_{\mathcal{N}} = \frac{1}{(2\pi)^{|\mathbf{s}|/2} \cdot \sqrt{\det(\mathbf{C})}} \exp\left(-\frac{\beta^2(\mathbf{s}-\mathbf{s}_0)}{2}\right)$$

$$\beta^2(\mathbf{s}) = (\mathbf{s}-\mathbf{s}_0)^T \cdot \mathbf{C}^{-1} \cdot (\mathbf{s}-\mathbf{s}_0)$$

- Gaussian distribution of statistical parameters with mean $\mathbf{s}_0$ and covariance $\mathbf{C}$

Fresh yield analysis [Graeb 2007]

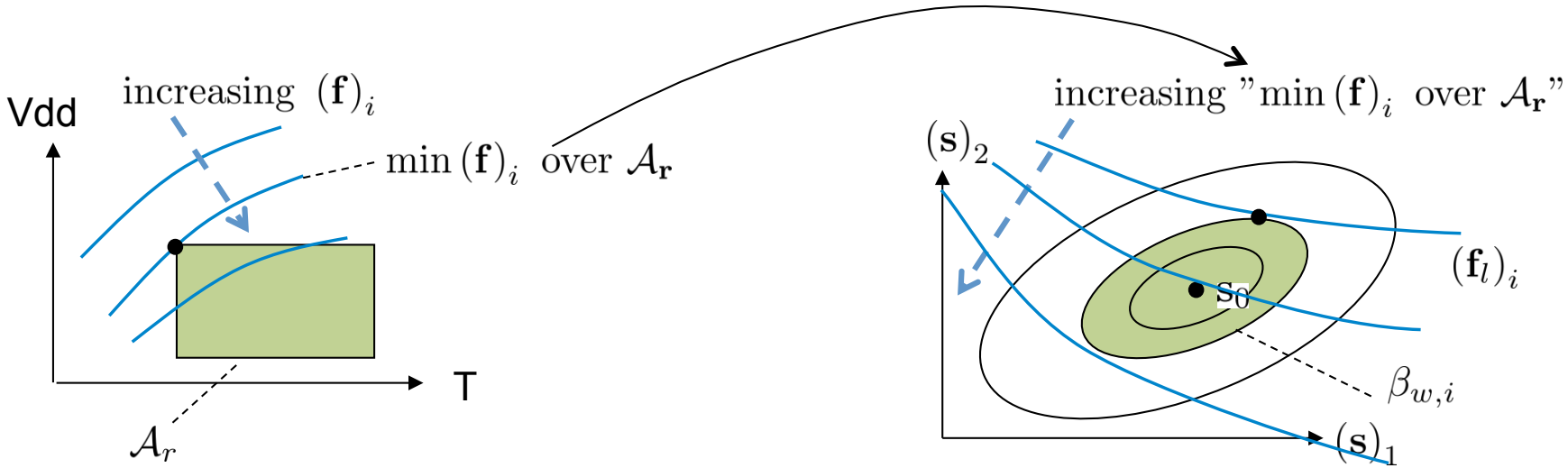




$$\mathcal{A}_\mathbf{r} = \left\{ \begin{bmatrix} \mathrm{T} \\ \mathrm{Vdd} \end{bmatrix} \middle| \begin{matrix} \mathrm{T}_{\mathrm{min}} \leq \ \mathrm{T} \ \leq \mathrm{T}_{\mathrm{max}} \ \wedge \\ \mathrm{Vdd}_{\mathrm{min}} \leq \mathrm{Vdd} \leq \mathrm{Vdd}_{\mathrm{max}} \end{matrix} \right\}$$

- Gaussian distribution of statistical parameters with mean $\mathbf{s}_0$ and covariance $\mathbf{C}$
- Tolerance box for the operating parameters

Fresh yield analysis [Graeb 2007]

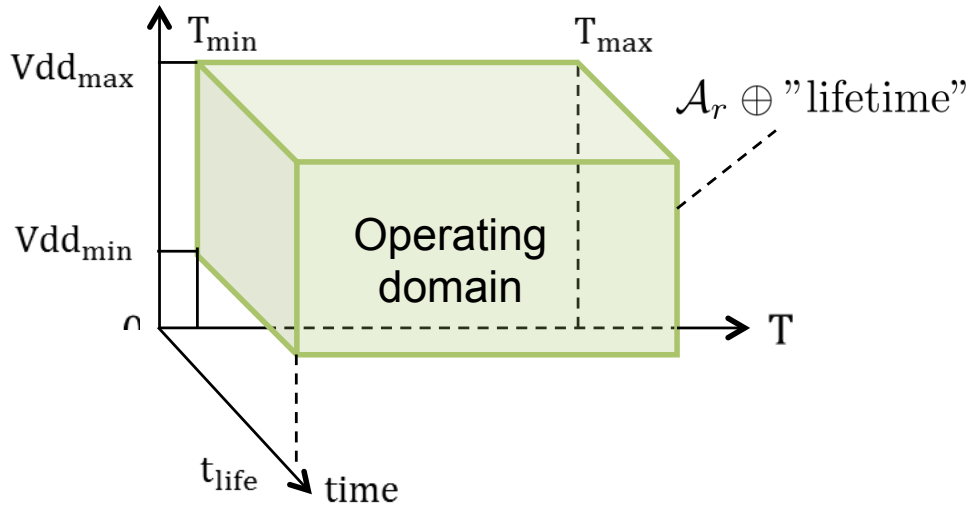


- Fresh yield analysis: $\min_{\mathbf{s}} \beta^2(\mathbf{s})$ s.t. $\left(\min_{\mathbf{r} \in \mathcal{A}_\mathbf{r}} (\mathbf{f})_i\right) \leq (\mathbf{f}_l)_i \xrightarrow[\text{gives}]{\text{solving}} \beta_{w,i}^2$
- Bijective mapping bwtween $\beta_{w,i}$ and yield: $\bar{Y}_{\text{fresh},i} = \int_{-\infty}^{\beta_{w,i}} \frac{1}{\sqrt{2\pi}} \exp\left(-\frac{1}{2}\xi^2\right) d\xi$
-

β_w	-1	0	1	2	3	4
$\bar{Y}$	15.9%	50%	84.1%	97.7%	99.9%	99.99%

Lifetime yield analysis

- Extend the domain of operating parameters with a circuit lifetime



- Lifetime yield analysis becomes

$$\min_{\mathbf{s}} \beta^2(\mathbf{s}) \text{ s.t. } \left(\min_{\substack{\mathbf{r} \in \mathcal{A}_\mathbf{r} \wedge \\ 0 \le t \le t_{\text{life}}}} (\mathbf{f})_i \right) \le (\mathbf{f}_l)_i \xrightarrow[\text{gives}]{\text{solving}} \beta^2_{w,i}$$

$$\bar{Y}_{\text{life},i} = \int_{-\infty}^{\beta_{w,i}} \frac{1}{\sqrt{2\pi}} \exp\left(-\frac{1}{2}\xi^2\right) d\xi$$

- Incremental cost is the cost of an additional operating parameter

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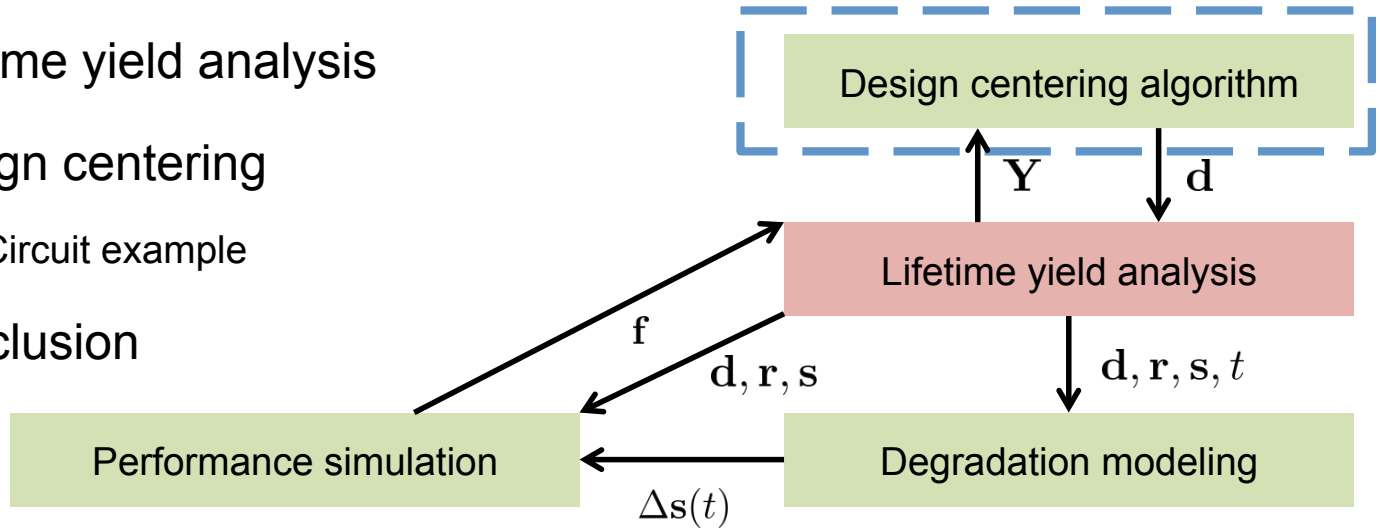
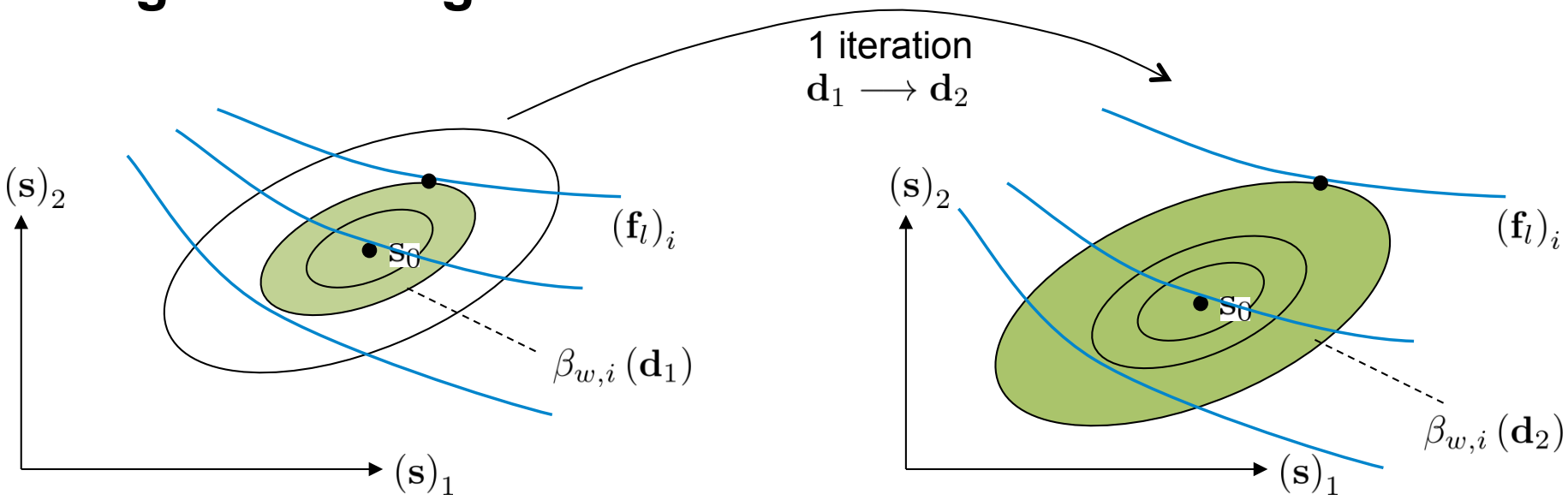


Design centering



- $\beta_{w,i}$ is a function of the design parameters $\mathbf{d}$
- Design centering formulation

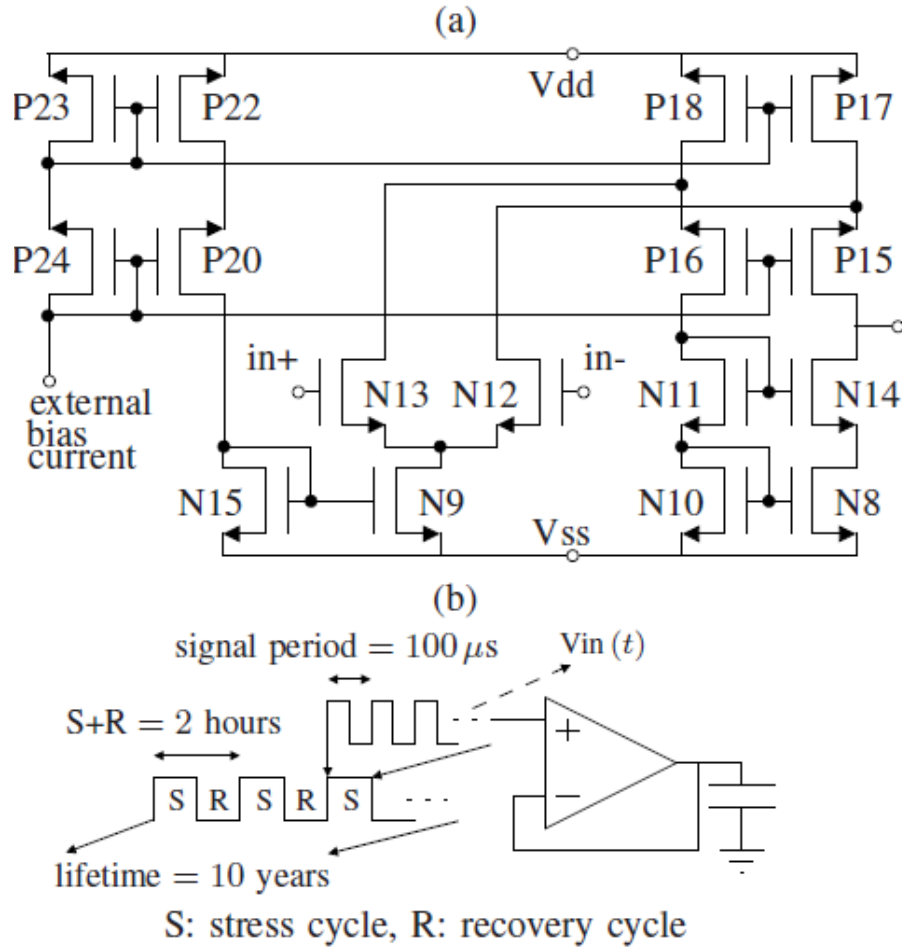
$$\mathbf{d}_{\text{solution}} = \arg\max_{\mathbf{d}} \min_{1 \leq i \leq |\mathbf{f}|} \beta_{w,i}(\mathbf{d})$$

- Terminate when yield is satisfactory or no new step is possible

Design centering – circuit example

- 39 process parameters
- 33 design parameters
- Operating parameter ranges

$$
\begin{array}{ccccc}
0 & \leq & \mathrm{T} & \leq & 110 \quad {}^{\circ}C \\
1.8 & \leq & \mathrm{Vdd} & \leq & 2.2 \quad \mathrm{V} \\
0 & \leq & \mathrm{mag}\{\mathrm{Vin}\} & \leq & 0.4 \quad \mathrm{V} \\
0 & \leq & t & \leq & 10 \quad \mathrm{years}
\end{array}
$$



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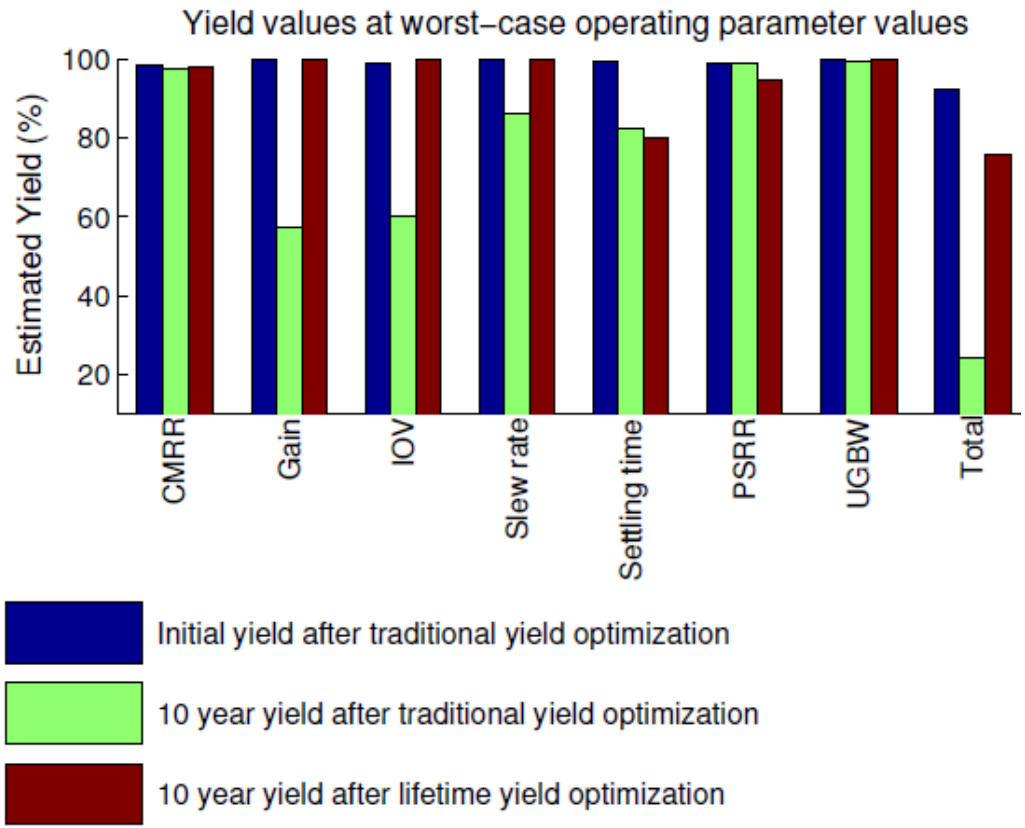
\end{array}
$$

- Specifications

60 dB	<	CMRR		
80 dB	<	Gain		
1.5 mV	<	IOV	<	1.5 mV
5 V/us	<	Slew rate		
60 dB	<	PSRR		
7 MHz	<	UGBW		



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- Cost in CPU time (hours)
- For lifetime yield analysis:
  - ~ 1000 Performance simulations
  - ~ 3000 Degradation simulations

	Fresh yield optimization	Lifetime yield optimization
Performance simulation	1.6	3.7
Degradation modeling	N/A	15.1

Initial yield after traditional yield optimization

10 year yield after traditional yield optimization

10 year yield after lifetime yield optimization

Design centering – circuit example

- 39 process parameters
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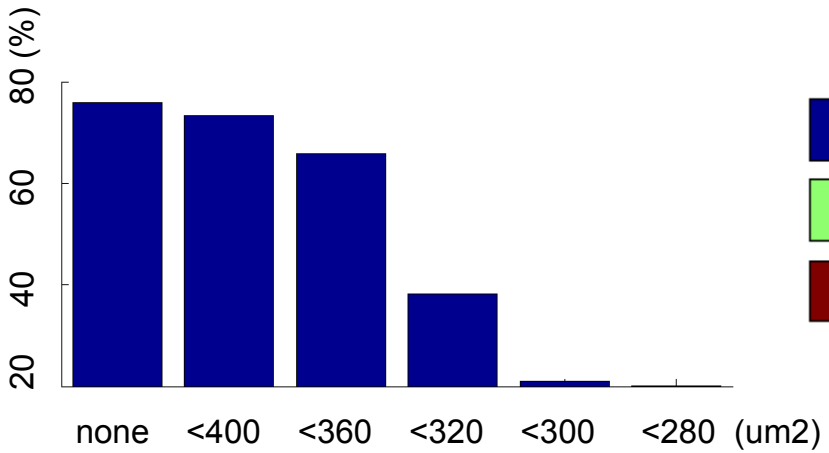
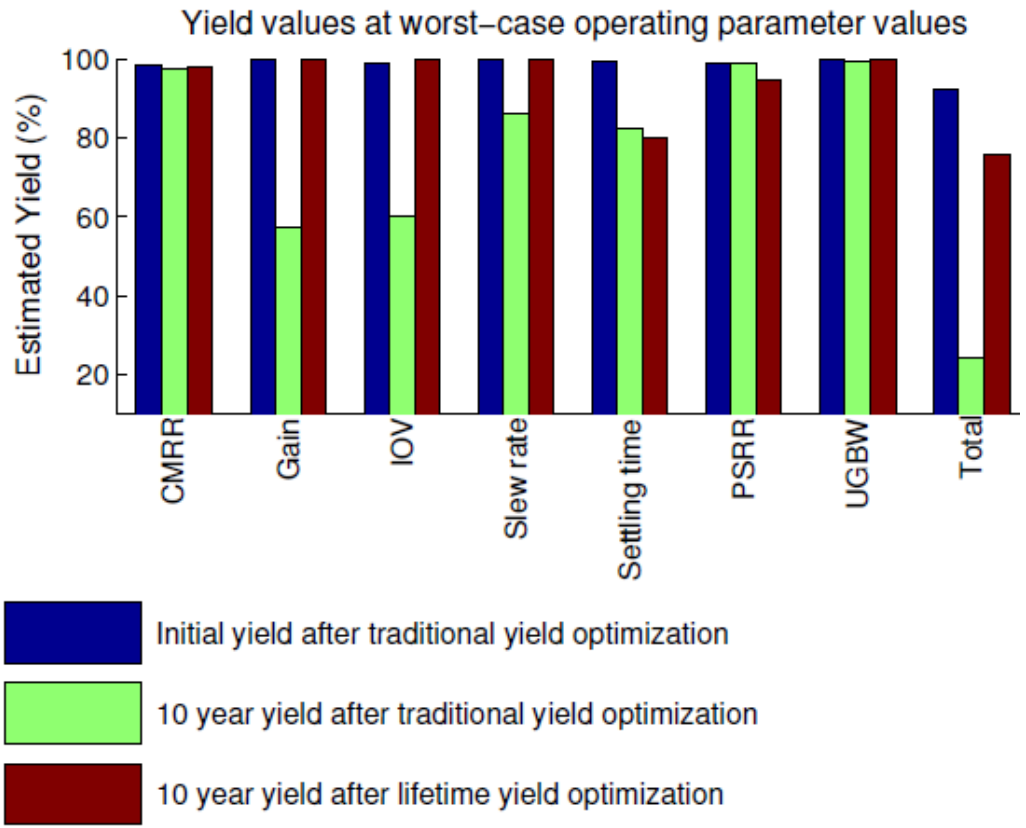
- Operating parameter ranges

$$\begin{array}{rcccl} 0 & \leq & \mathrm{T} & \leq & 110 \quad {}^{\circ}C \\ 1.8 & \leq & \mathrm{Vdd} & \leq & 2.2 \quad \mathrm{V} \\ 0 & \leq & \mathrm{mag}\{\mathrm{Vin}\} & \leq & 0.4 \quad \mathrm{V} \\ 0 & \leq & t & \leq & 10 \quad \mathrm{years} \end{array}$$

- Multi-objective optimization
  - Yield versus circuit area





Conclusion

- NBI degradation model suitable for analog circuit design
- Decoupling of degradation and performance simulation [ICICDT 2013]
- Simple extension to calculate lifetime yield analysis
- Demonstration on a circuit example

Future work

- New circuit examples

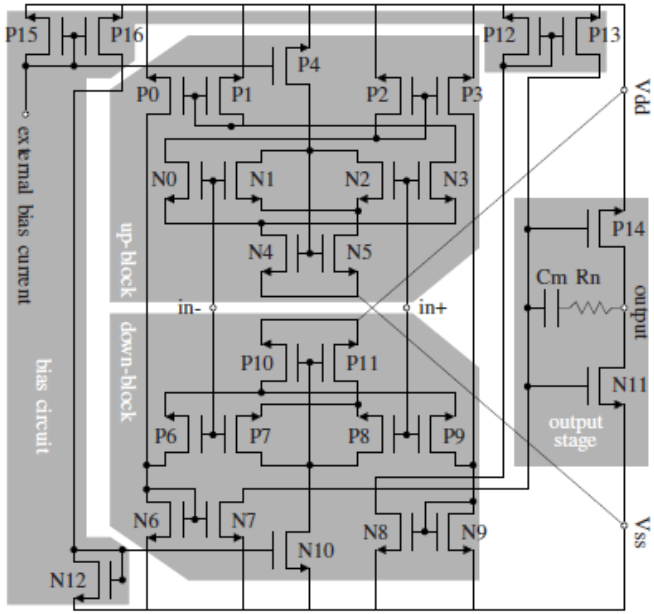


Fig. 1. Rail-to-rail operational amplifier.

Backup slides

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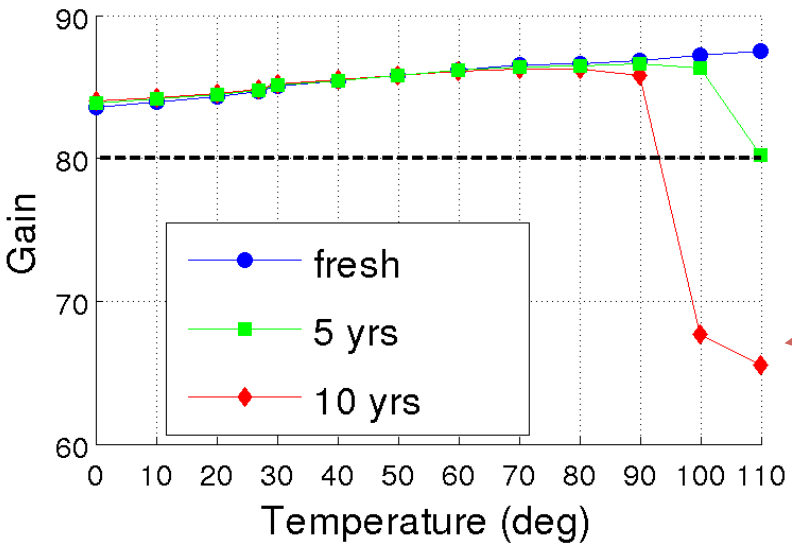
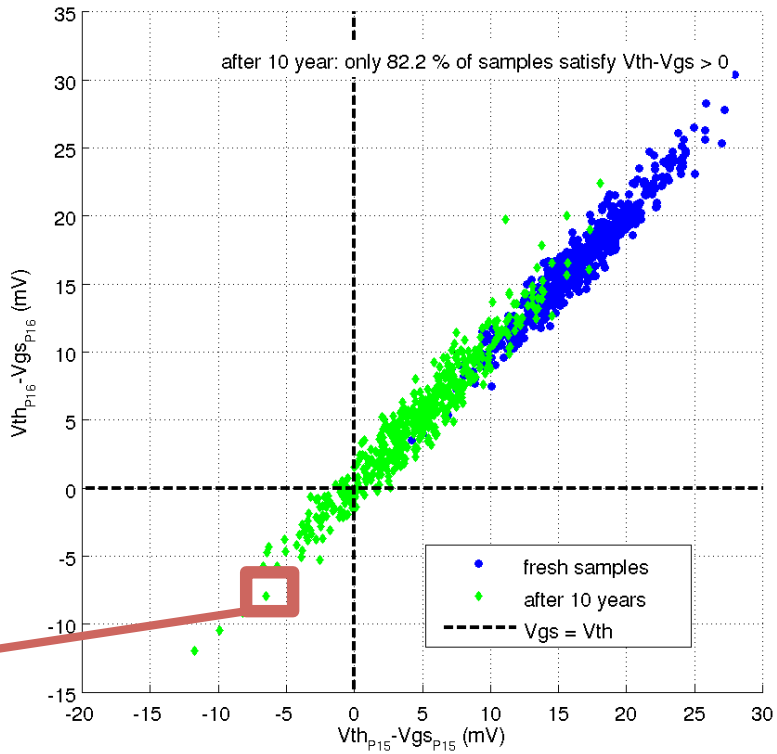
Significance of lifetime sizing rules

- Define the feasible region of operation
- Aid optimization and reduce cost
- Typically sharp changes in the performance functions will be avoided





Background

- Variation in $\Delta \mathrm{Vth}$ observed at (at least) three different time scales

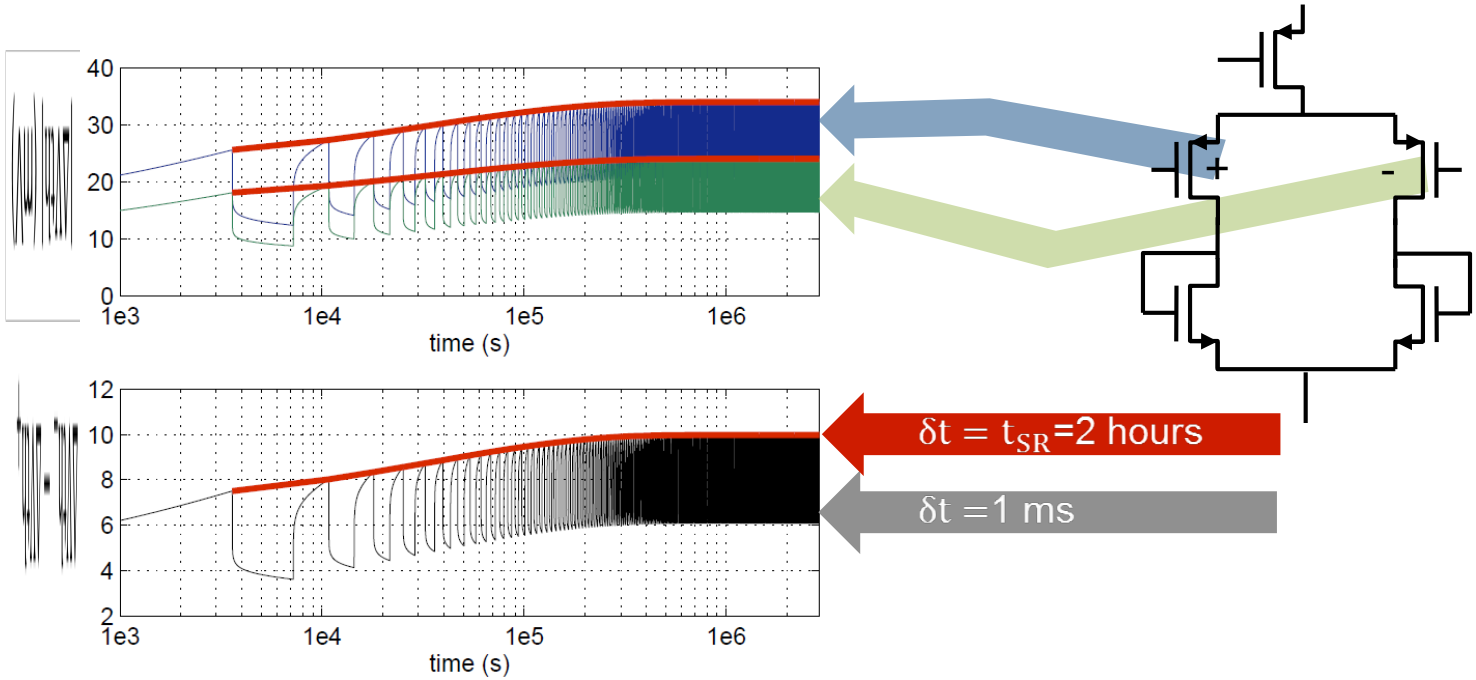
- Scale of large signals, transient response to input stimulus, *small* stress and recovery time constants.
  - Large signals cause a significant change in $\mathrm{Vgs(t)}$
  - The change typically has a period in ns to μs
  - $\tau_{s1} = 1\,ms$, $\tau_{r1} = 1\,\mu s$

- Scale of stress-and-recovery cycles
  - Recovery when the oxide electric field $\mathrm{E} = 0$
  - Rest cycles are in the length of, e.g., minutes to hours

- Long-term increase in the envelope of $\Delta \mathrm{Vth}$
  - Significant over days to years

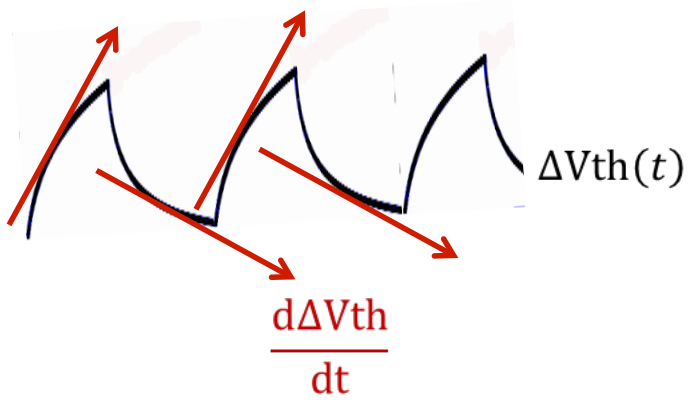
Problems

- Tradeoff between computational cost and the number of simulation steps
  - Small simulation step (δt) due to the difference between time scales
  - In the previous example, number of steps $= \frac{t_{life}}{\delta t} = \frac{100\ \text{days}}{1\ \text{ms}} = 8.64E9$
  - Ignoring the smaller time scales leads to error, e.g., mismatch error



Problems

- Tradeoff between computational cost and the number of simulation steps
- Degradation modeling and performance evaluation are coupled
- Issues using gradient-based numerical algorithms
  - $\frac{\mathrm{df}}{\mathrm{dt}} = \frac{\partial \mathbf{f}}{\partial \mathrm{t}} + \frac{\partial \mathbf{f}}{\partial \mathrm{Vth}} \cdot \frac{\mathrm{d\Delta Vth}}{\mathrm{dt}}$; $\frac{\mathrm{d\Delta Vth}}{\mathrm{dt}}$ flips sign in recovery cycles



New solutions

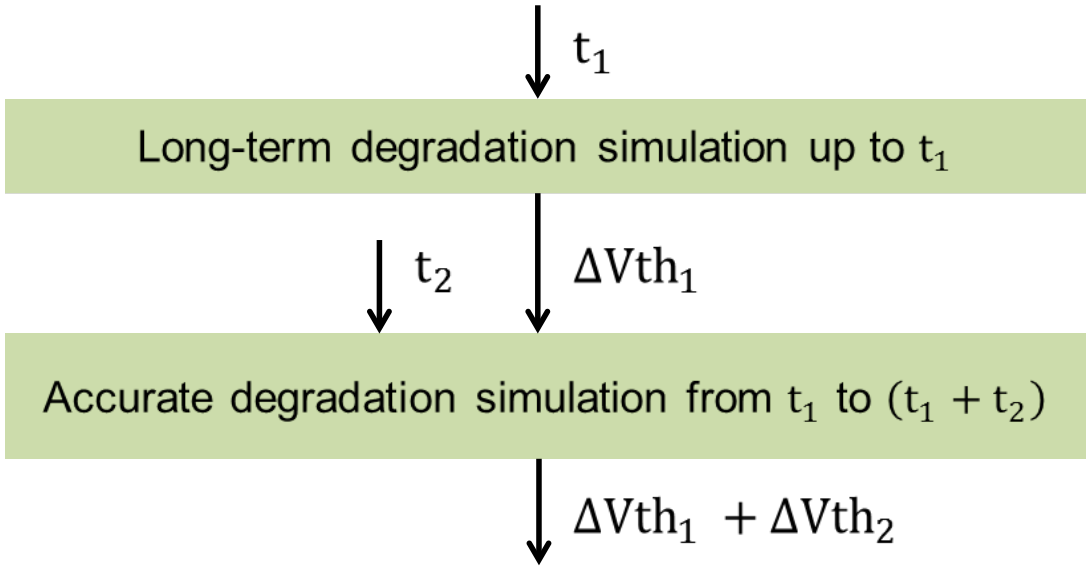
1. Rule to decouple degradation from performance simulation
2. Partition degradation simulation into long and short term components
   - $t = t_1 + t_2$
   - Long-term component $t_1 = M \cdot t_{SR}$
   - Short-term component $0 \leq t_2 \leq t_{SR}$

   - Coarse long-term model: $[0, t_1] \mapsto \Delta Vth_1(t_1)$
   - Accurate short-term model: $\{t_1, Vth_1(t_1), [0, t_2]\} \mapsto \Delta Vth_2(t_1, t_2)$

   - Components combination: $\Delta Vth(t_1 + t_2) \approx \Delta Vth_1(t_1) + \Delta Vth_2(t_1, t_2)$

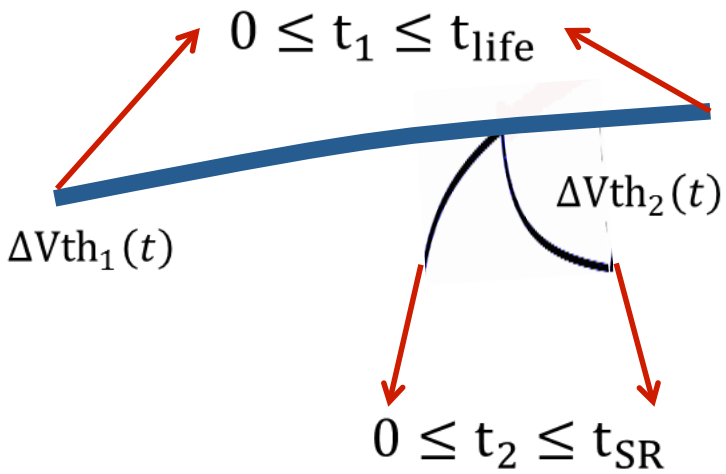
New solutions

1. Rule to decouple degradation from performance simulation
2. Partition degradation simulation into long and short term components
   - $t = t_1 + t_2$
   - Long-term component $t_1 = M \cdot t_{SR}$
   - Short-term component $0 \leq t_2 \leq t_{SR}$
   - Flowchart of calculation procedure



New solutions

1. Rule to decouple degradation from performance simulation
2. Partition degradation simulation into long and short term components
3. Extended domain of operating parameters
   - Two time dimensions, t_1 and t_2, are used in worst-case analysis
   - Issue with the gradient sign flip is avoided



Conclusion

- Flowchart to evaluate a performance indicator as a function of time